CISPA
HELMHOLTZ CENTER FOR
INFORMATION SECURITY

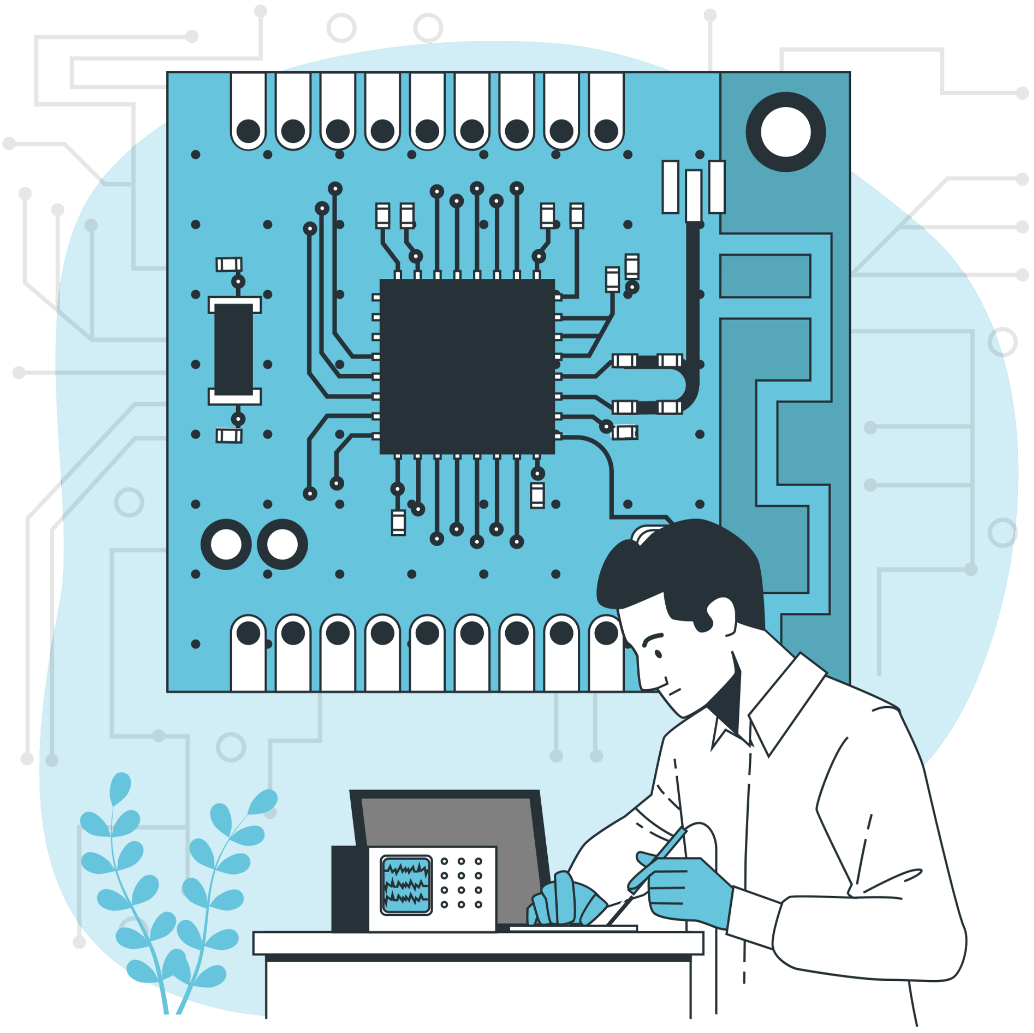
A Security RISC?

The State of Microarchitectural Attacks on RISC-V

Lukas Gerlach, **Daniel Weber**, Michael Schwarz | BlackHat EU 2023

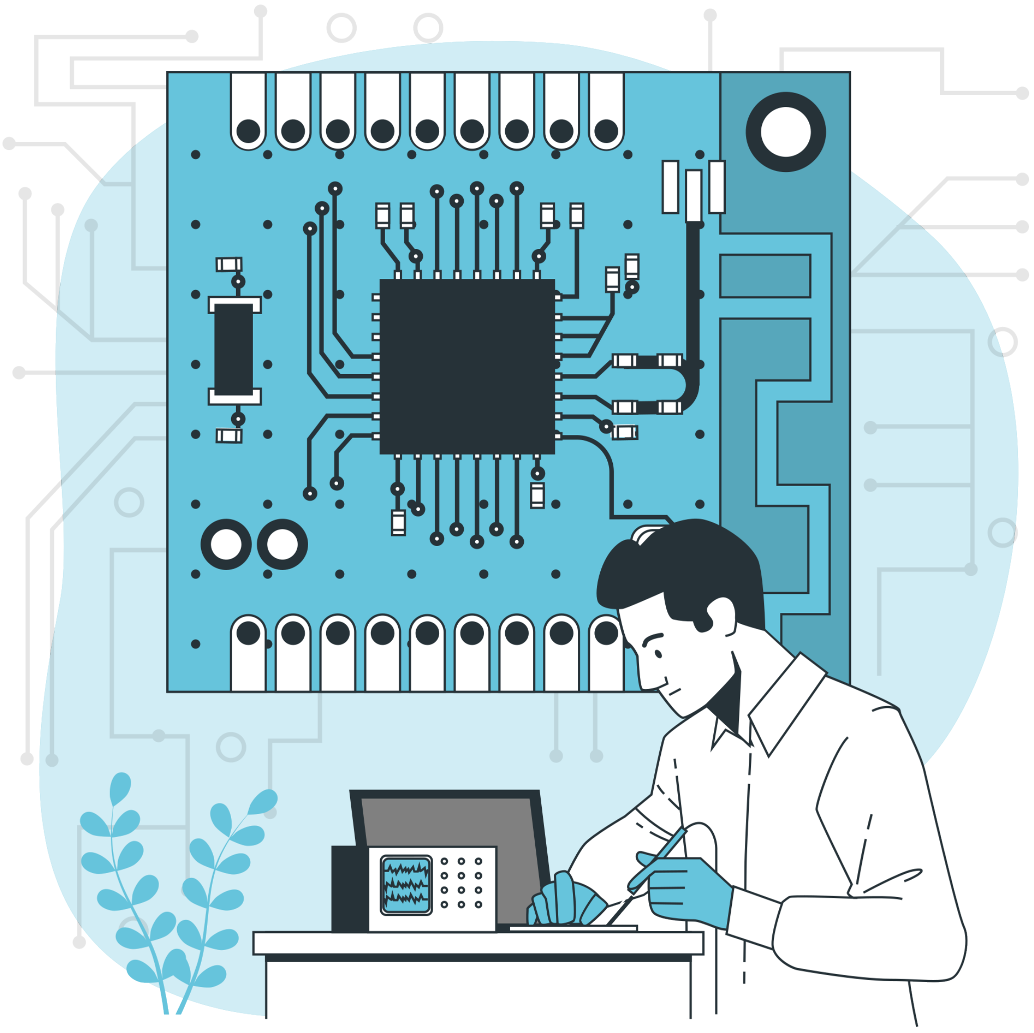
Agenda

Agenda



CPU Security Basics

Agenda



CPU Security Basics

Learn about existing Attacks

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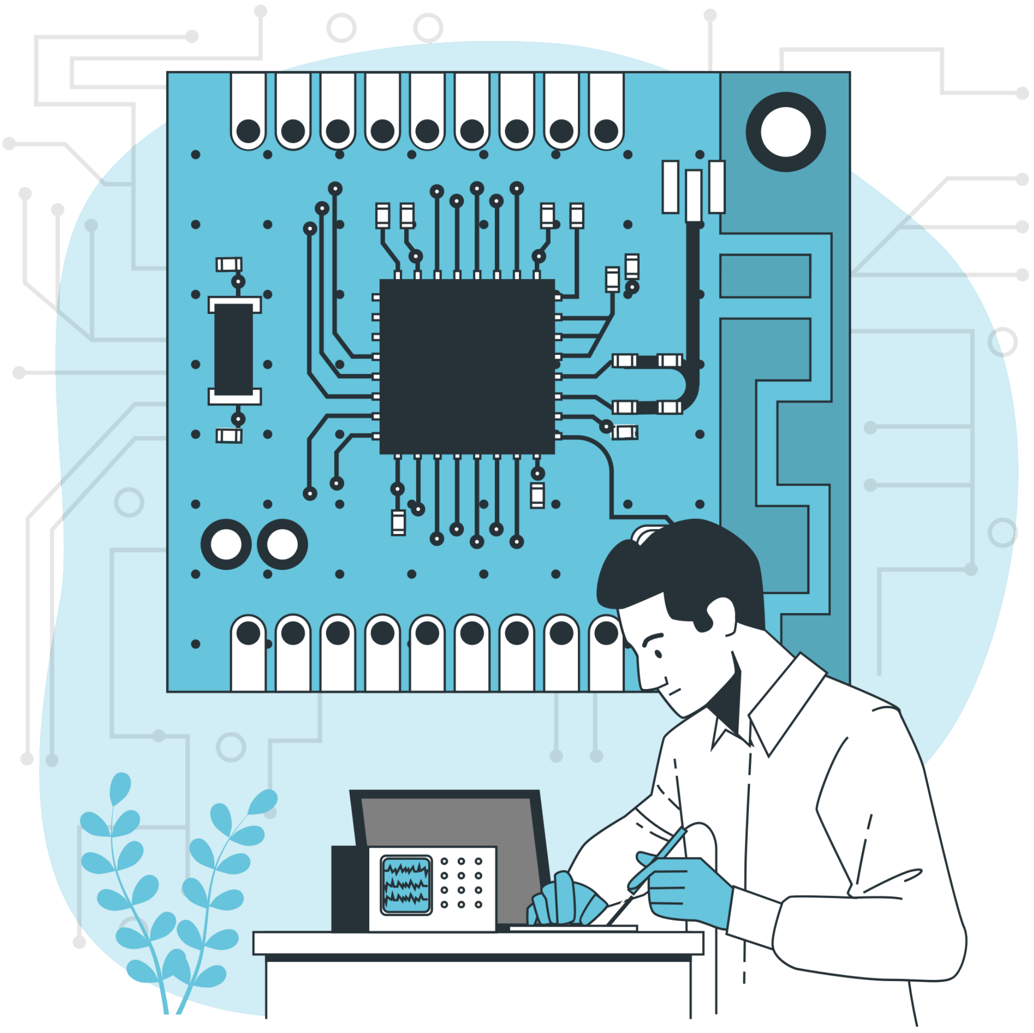

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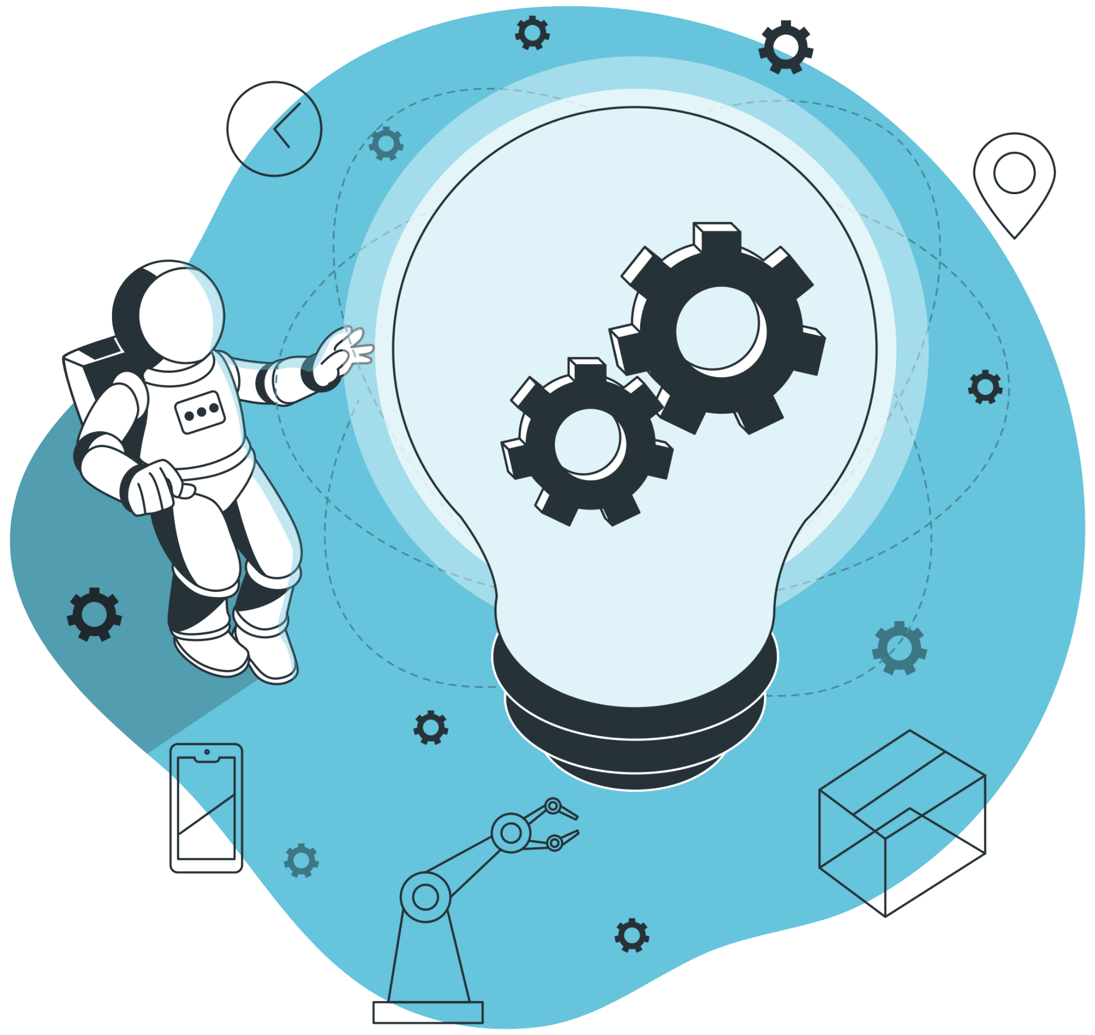

Investigate RISC-V Security

Who are we?

RootSec

Research Group

@

CISPA

Helmholtz Center for
Information Security

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Daniel Weber

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Michael Schwarz

Faculty

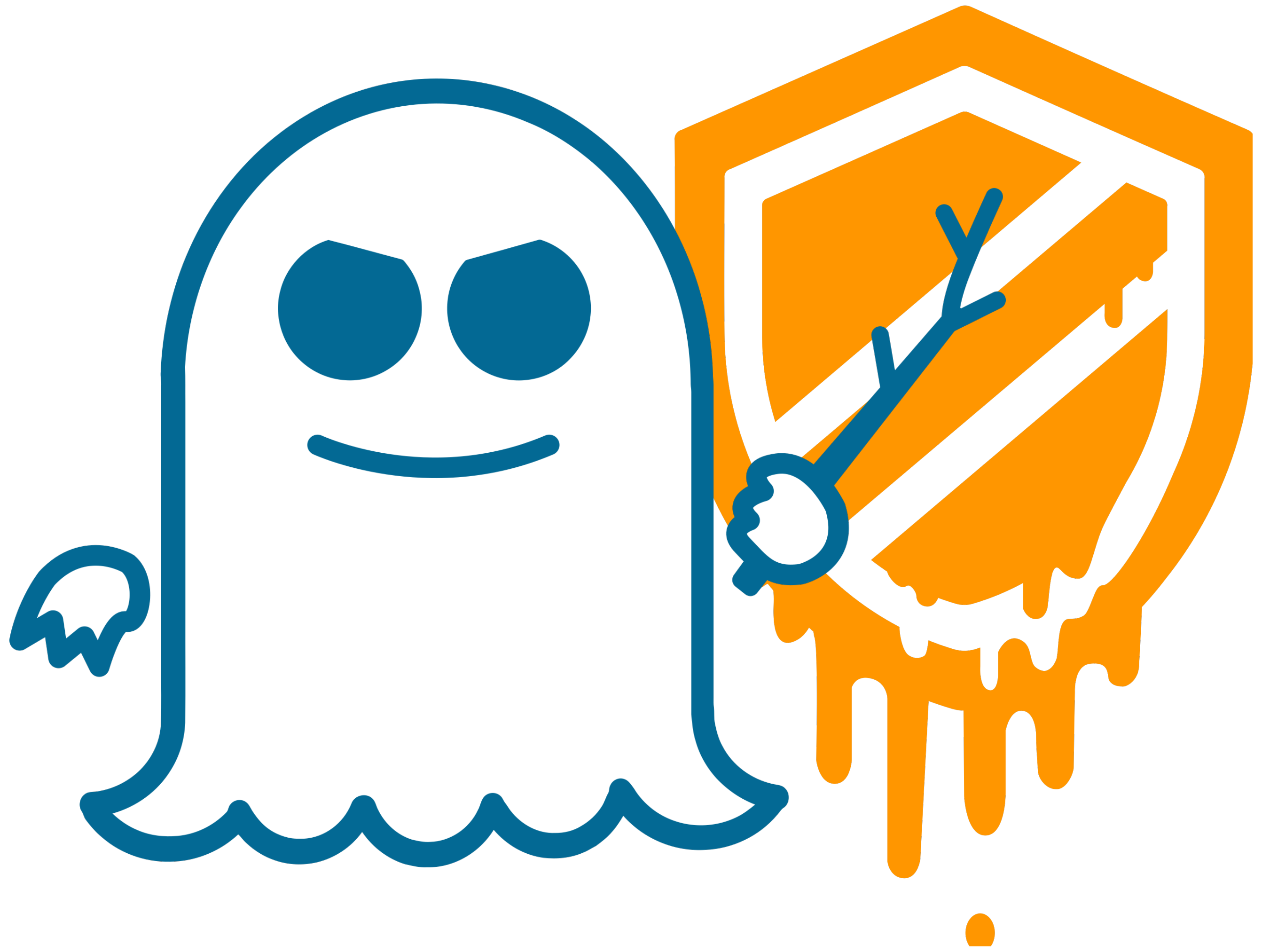
Why do we Care about CPU Security?

Live Demo

demo@lab24: ~/demos
⌥⌘1

```
demo@lab24:~/demos$ ./leak
Calibrating Threshold
Cache hit timing: 5, Cache miss timing: 150
Threshold is: 101
```

Why do We Care about CPU Security?



Why do We Care about CPU Security?

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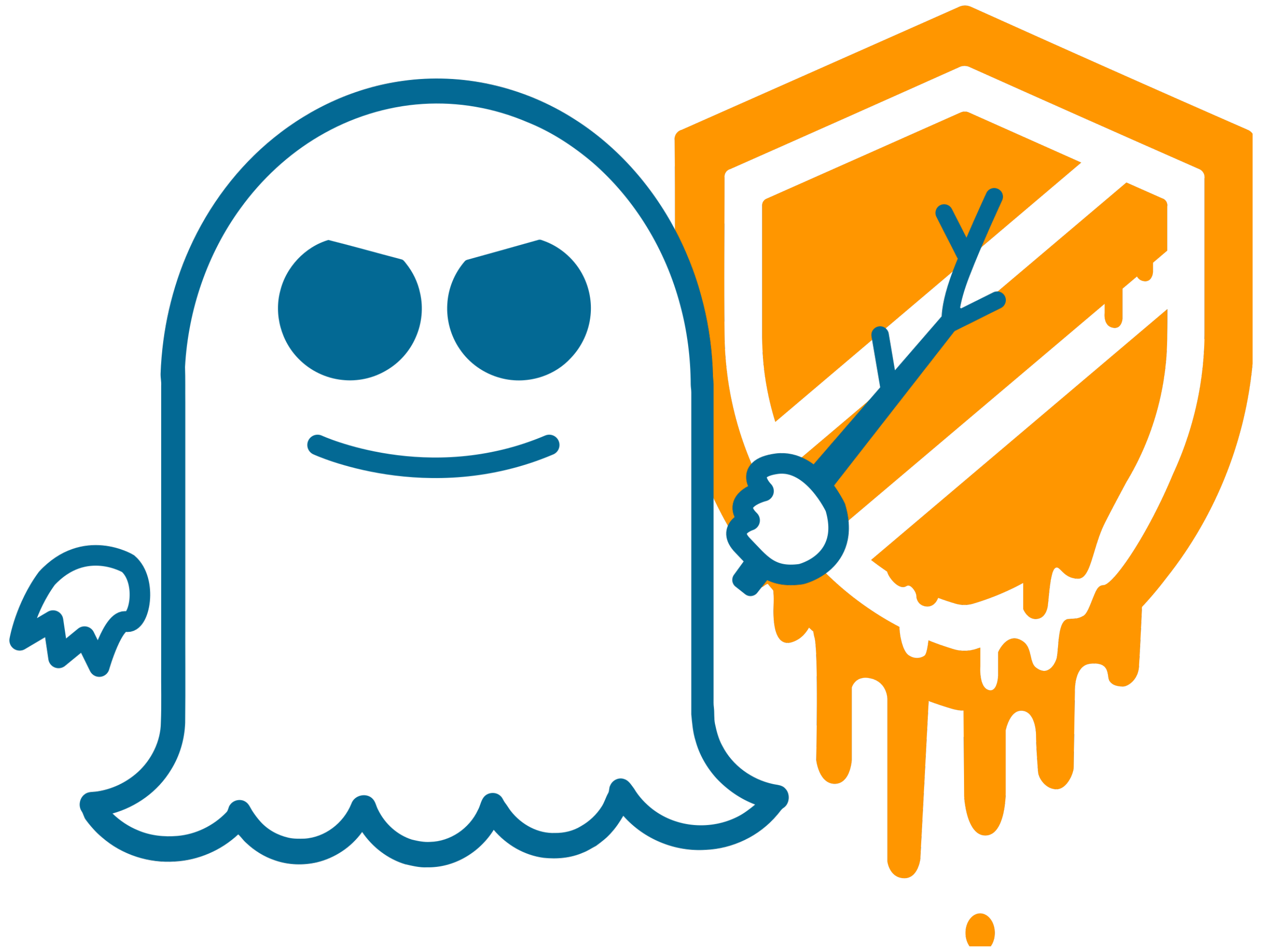

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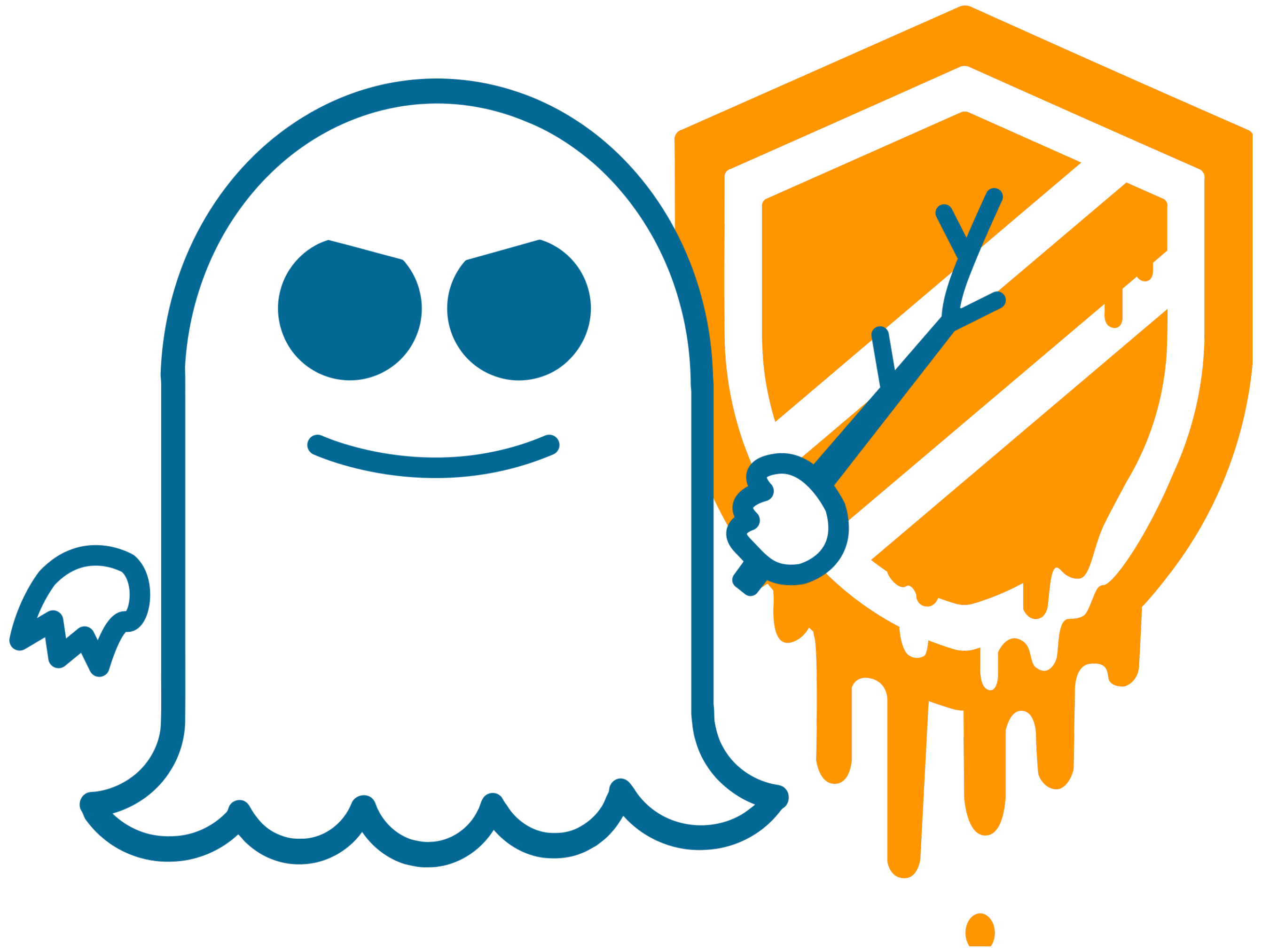

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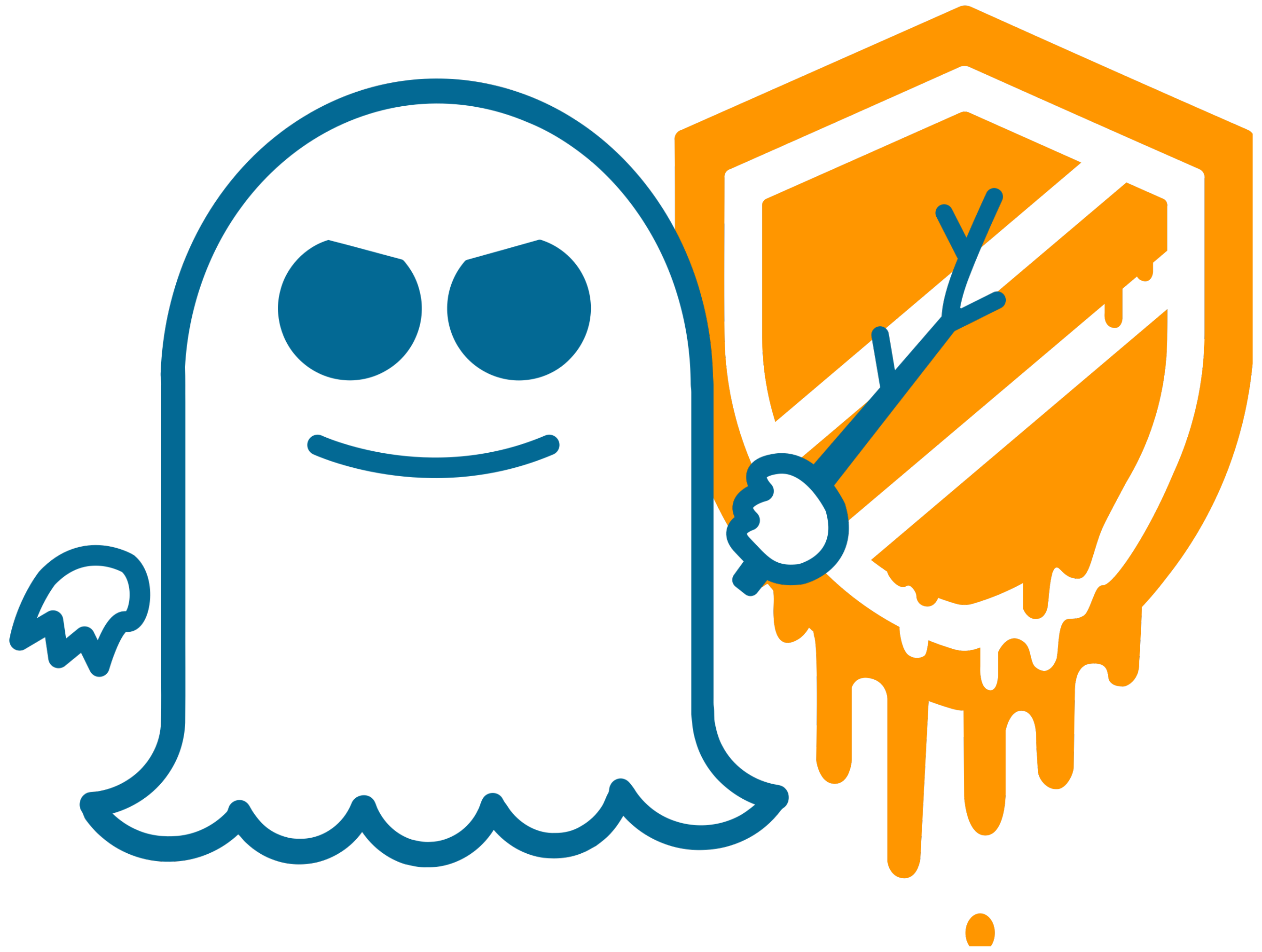

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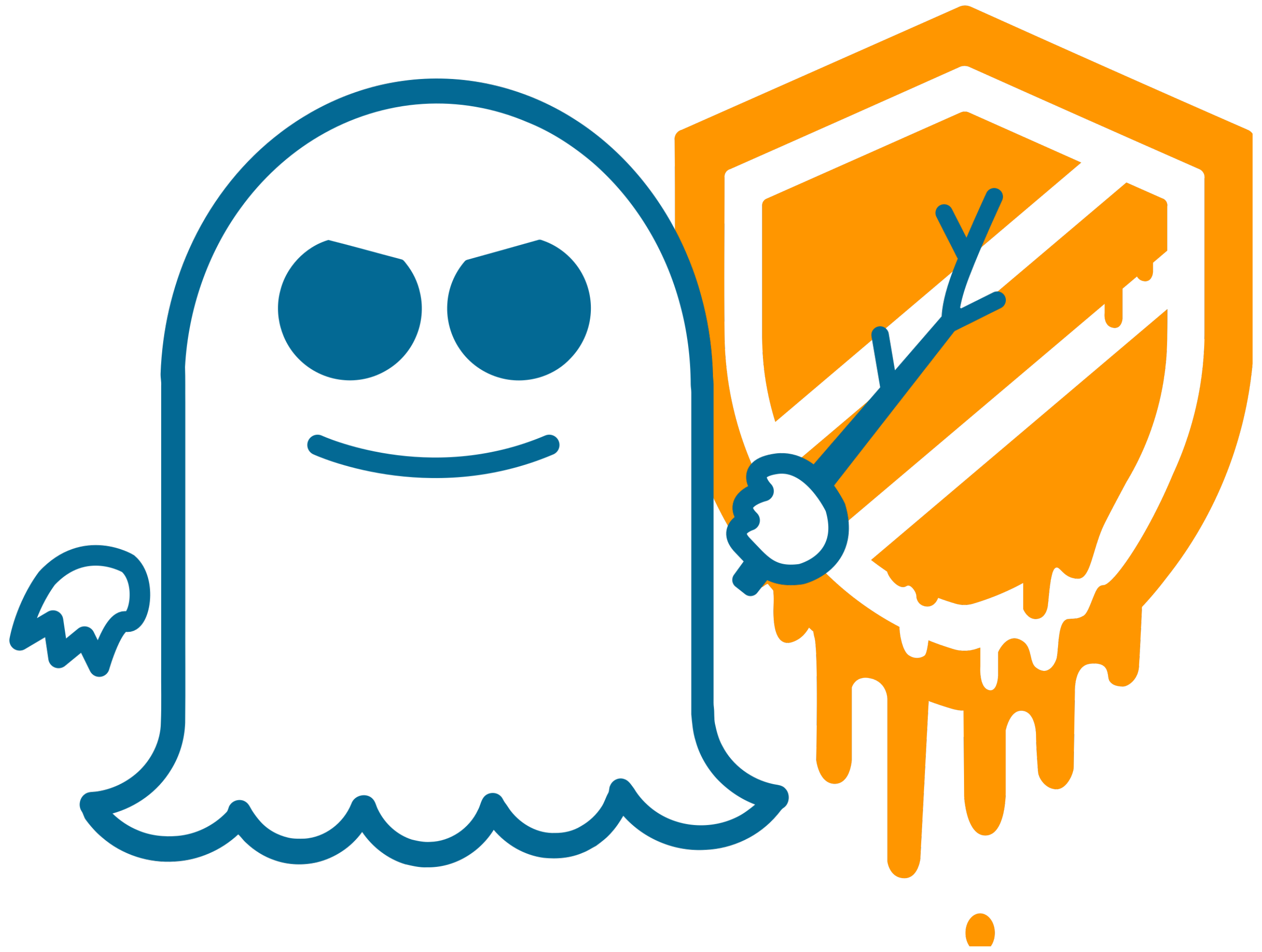

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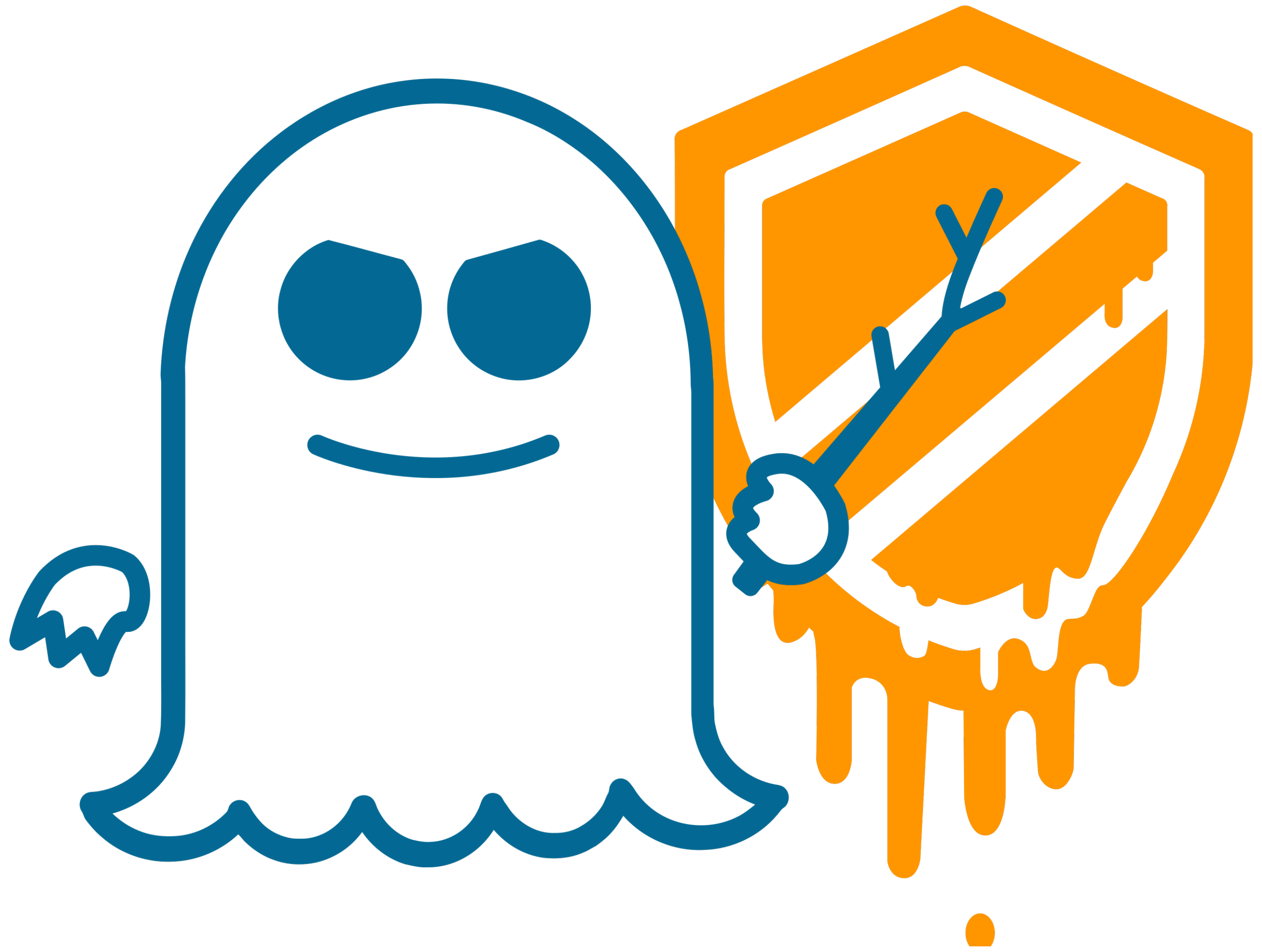

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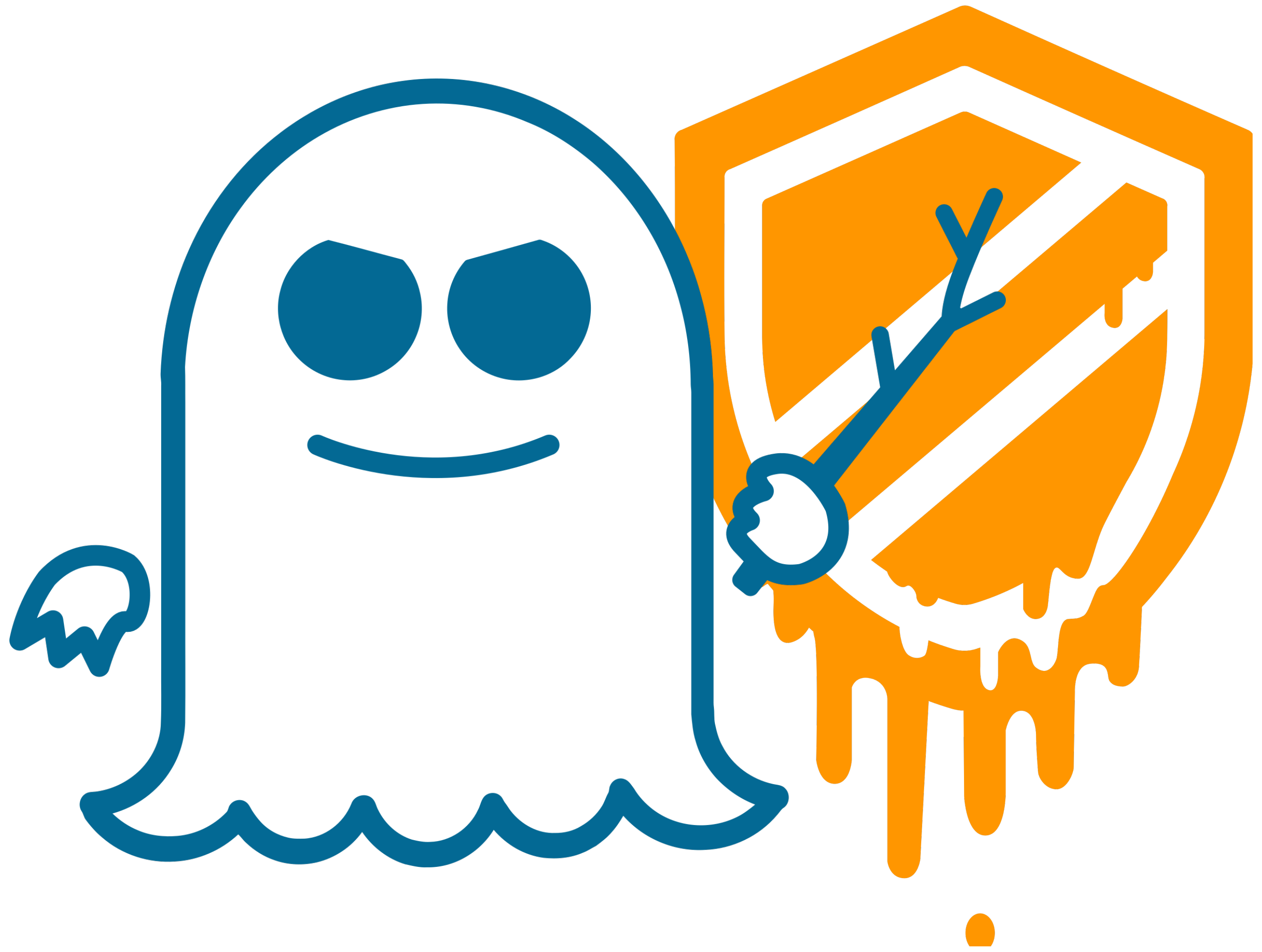

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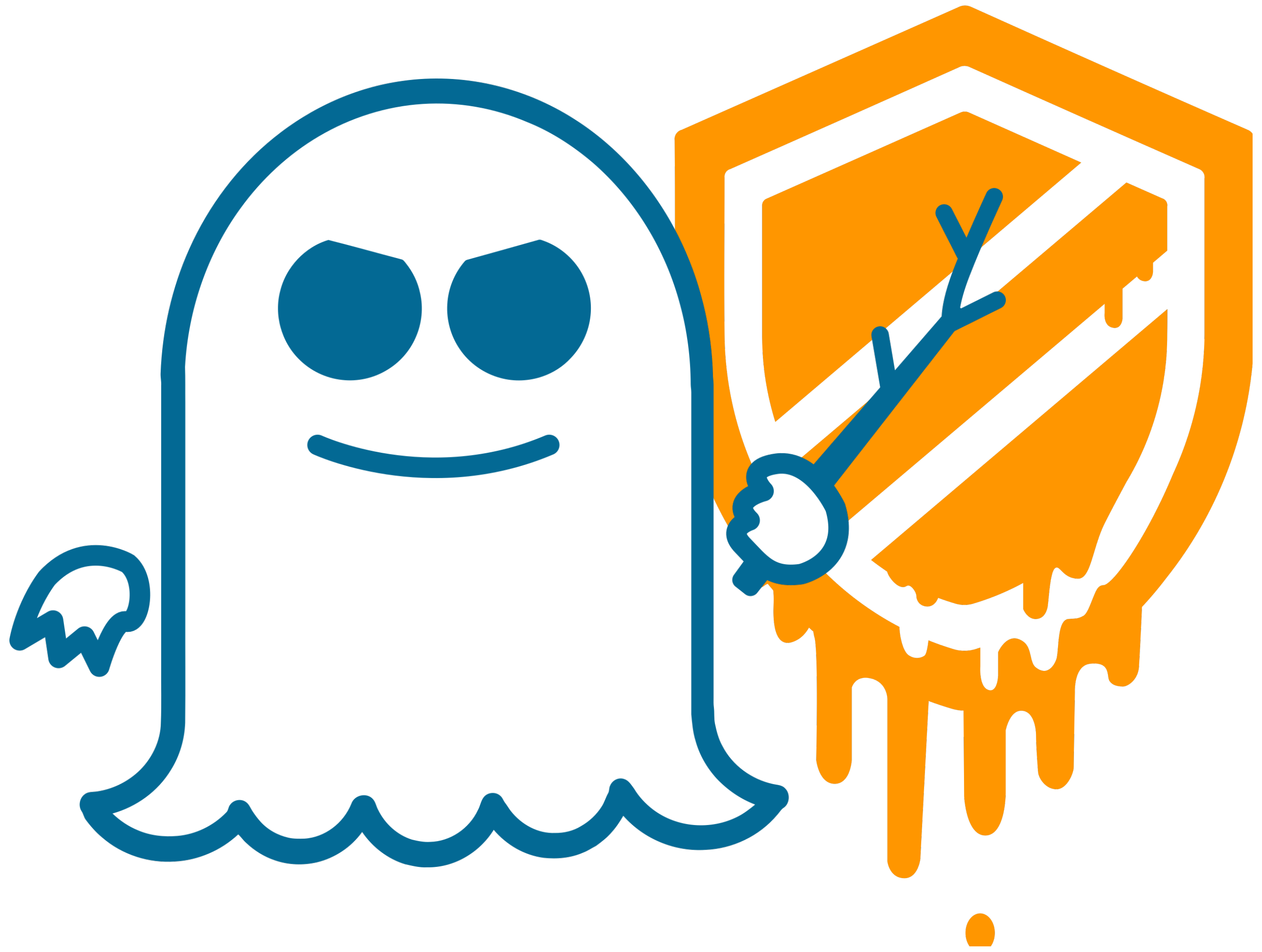

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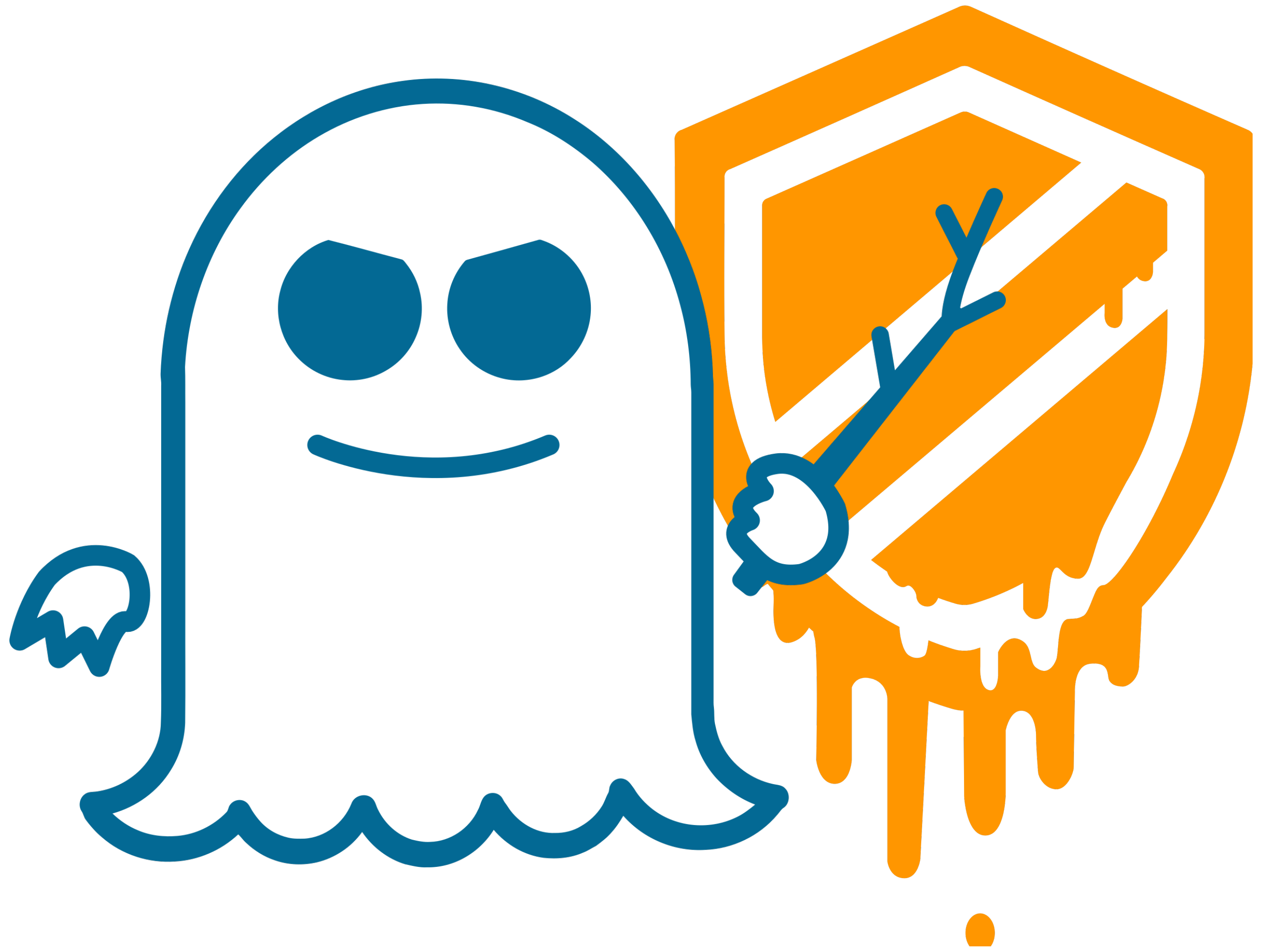

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MDS
PLUNDER
VOLT

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MD
S
PLUNDER
VOLT
ÆPIC
LEAK
iLeakage

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Why do We Care about CPU security?

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CACHE WARP

Different Vulnerabilities, Different Attacks

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- **Leaking Secrets:**

Different Vulnerabilities, Different Attacks

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Different Vulnerabilities, Different Attacks

- **Leaking Secrets:**
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  - CacheWarp
  - ...

Only Intel and AMD CPUs?

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What about the Others?

Other Architectures? ARM?

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- **Demonstrated attacks** include:
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→ **ARM is also vulnerable**

There is another!

RISC-V: The New Star on the Horizon

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- New **Instruction Set Architecture** (ISA)

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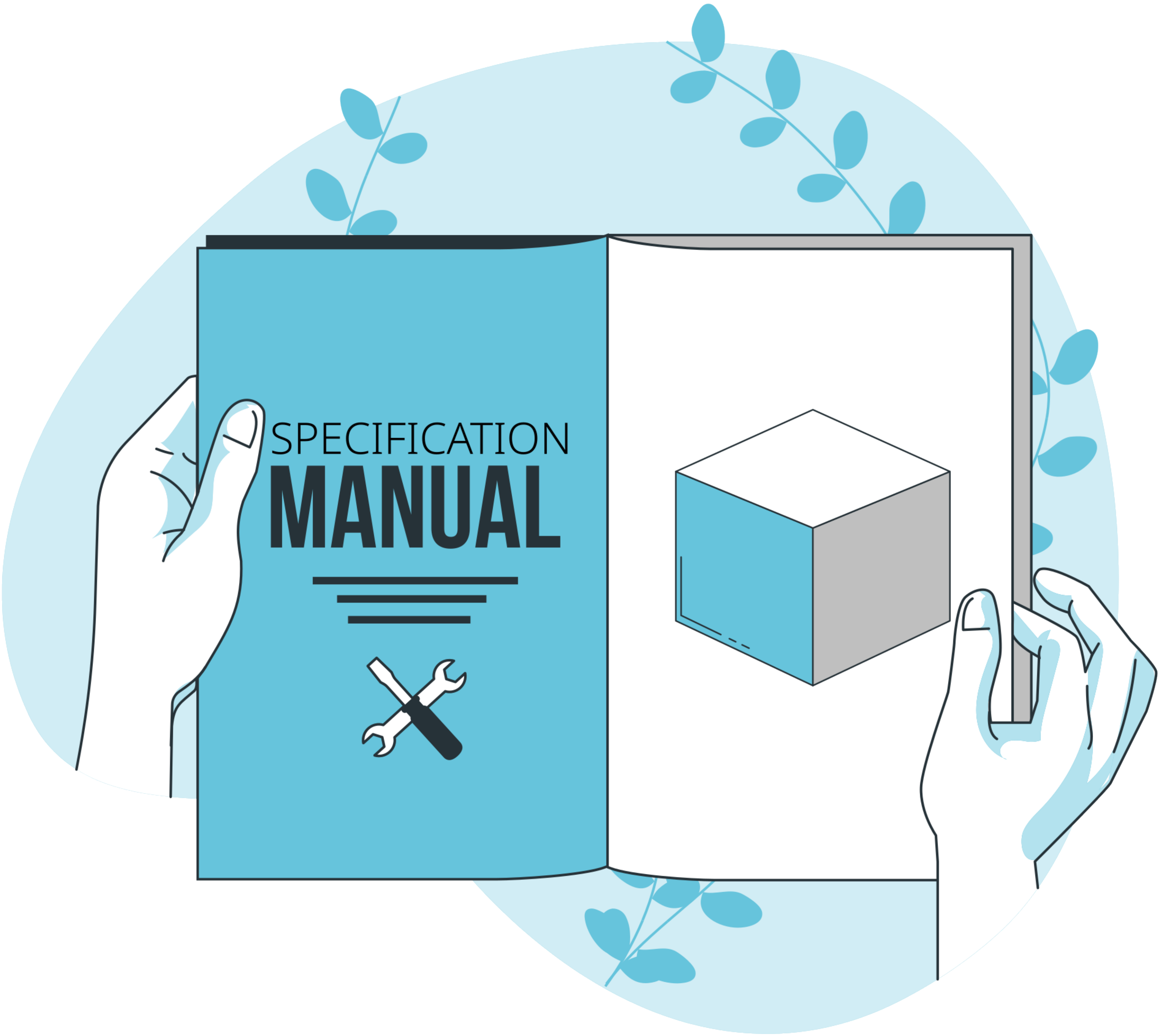
RISC-V: The New Star on the Horizon

- New **Instruction Set Architecture** (ISA)
- **Open-Source** Standard
  - White-box bug hunting
  - Testing of hardware mitigations
- Lots of **academic research**



Is RISC-V just another Academia Thingy?

You Can Buy RISC-V Cores!

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RISC-V®

Now available in Hardware

You Can Buy RISC-V Cores!

Allwinner D1 (C906)

Now available in Hardware

You Can Buy RISC-V Cores!

Allwinner D1 (C906)

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SiFive U74

RISC-V is Coming

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***62.4 billion** RISC-V cores predicted to be running*
by 2025

RISC-V is Coming

62.4 billion *RISC-V cores predicted to be running* ***by 2025***

*RISE Project by major vendors (**Google**, **Qualcomm**, **Samsung**, …)*

But Security?

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Security?

But Security?

Security?

What is the ***status quo*** *on*

hardware RISC-V processors*?*

Let’s Investigate RISC-V...

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Let’s Investigate RISC-V...

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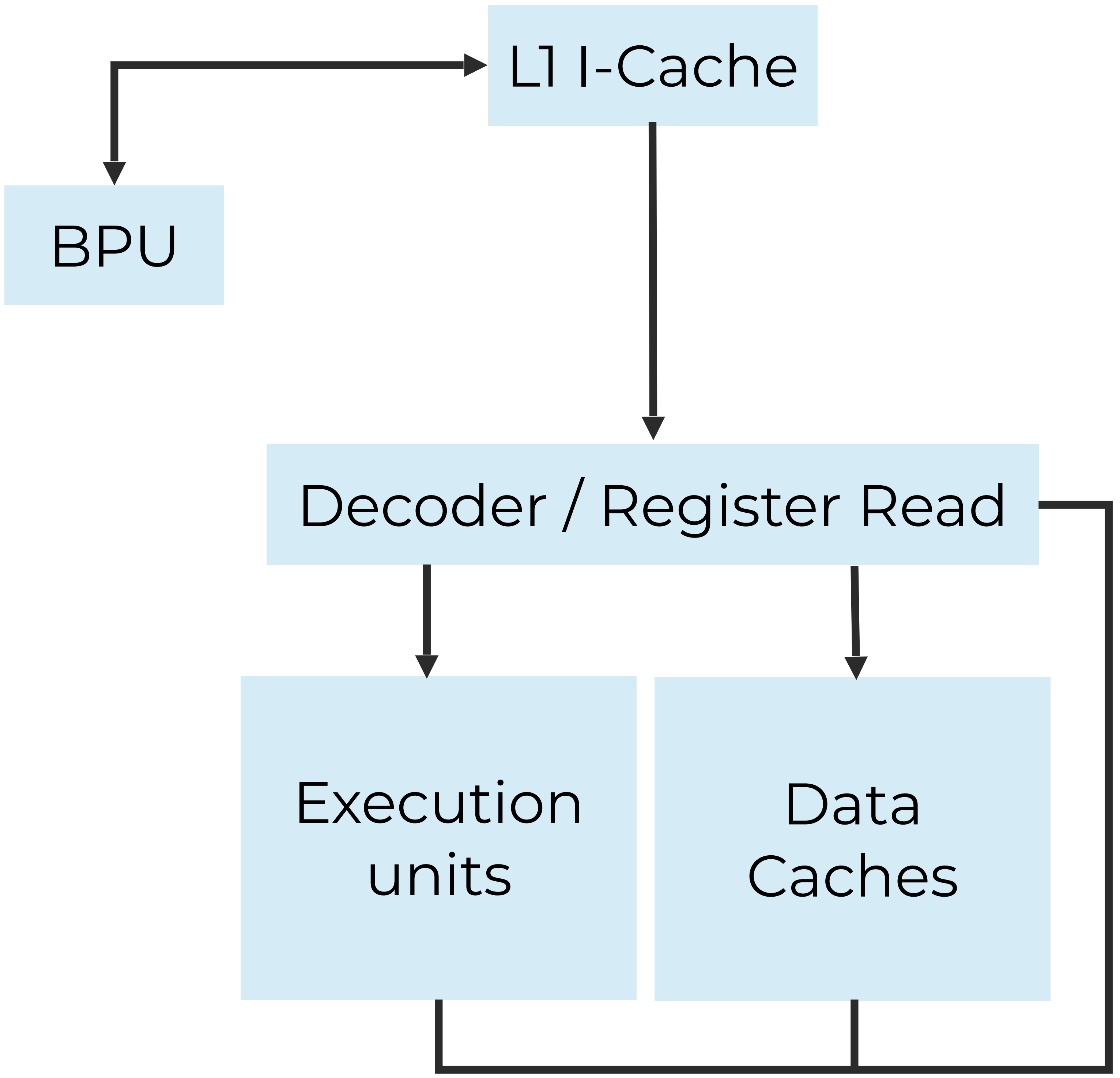
- Does **open-source imply better or worse** security?

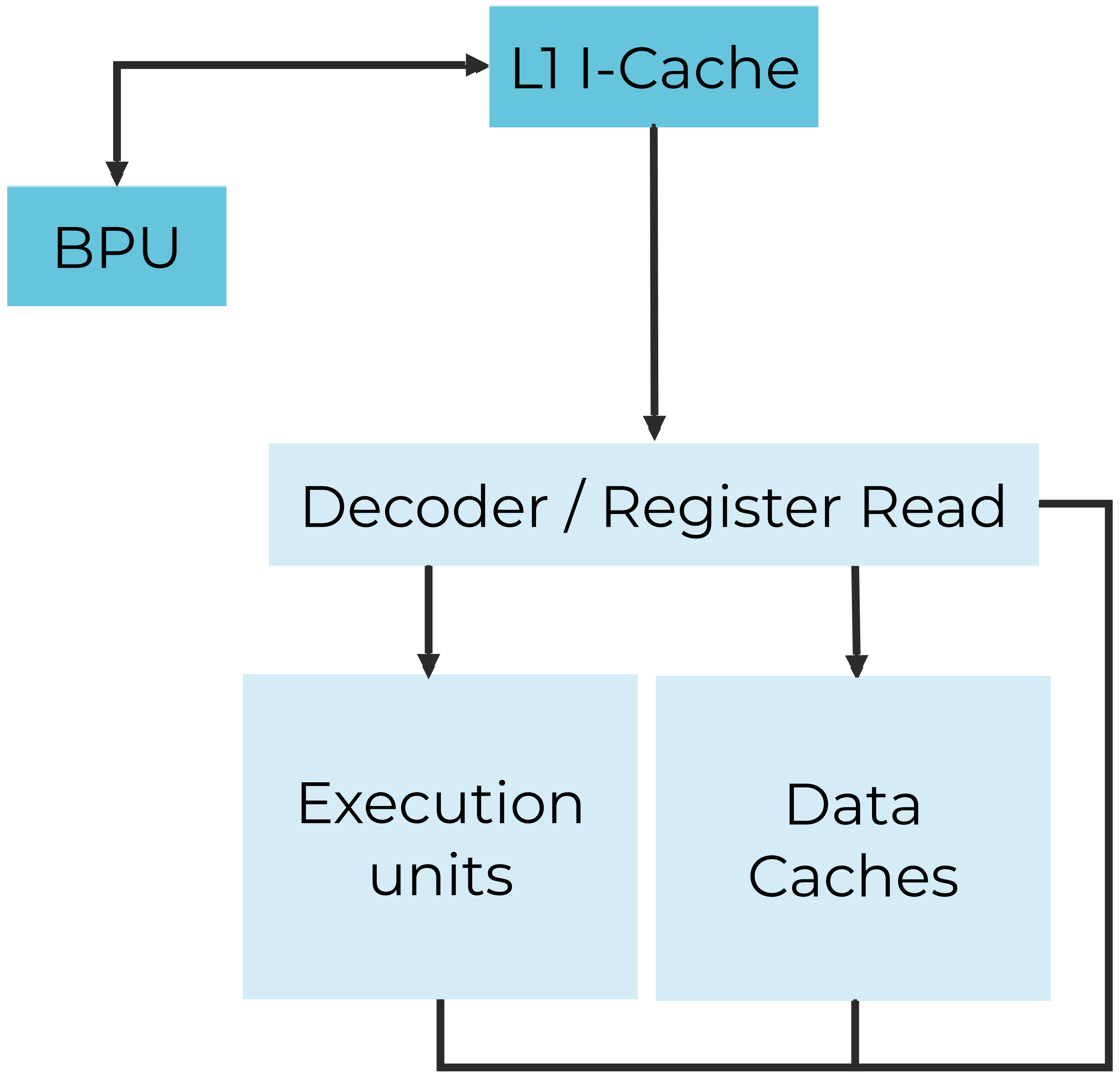
→ **Let’s analyze the C906 and U74!**

How Does a CPU Work?



How Does a CPU Work?

1. Fetch instruction from memory



How Does a CPU Work?

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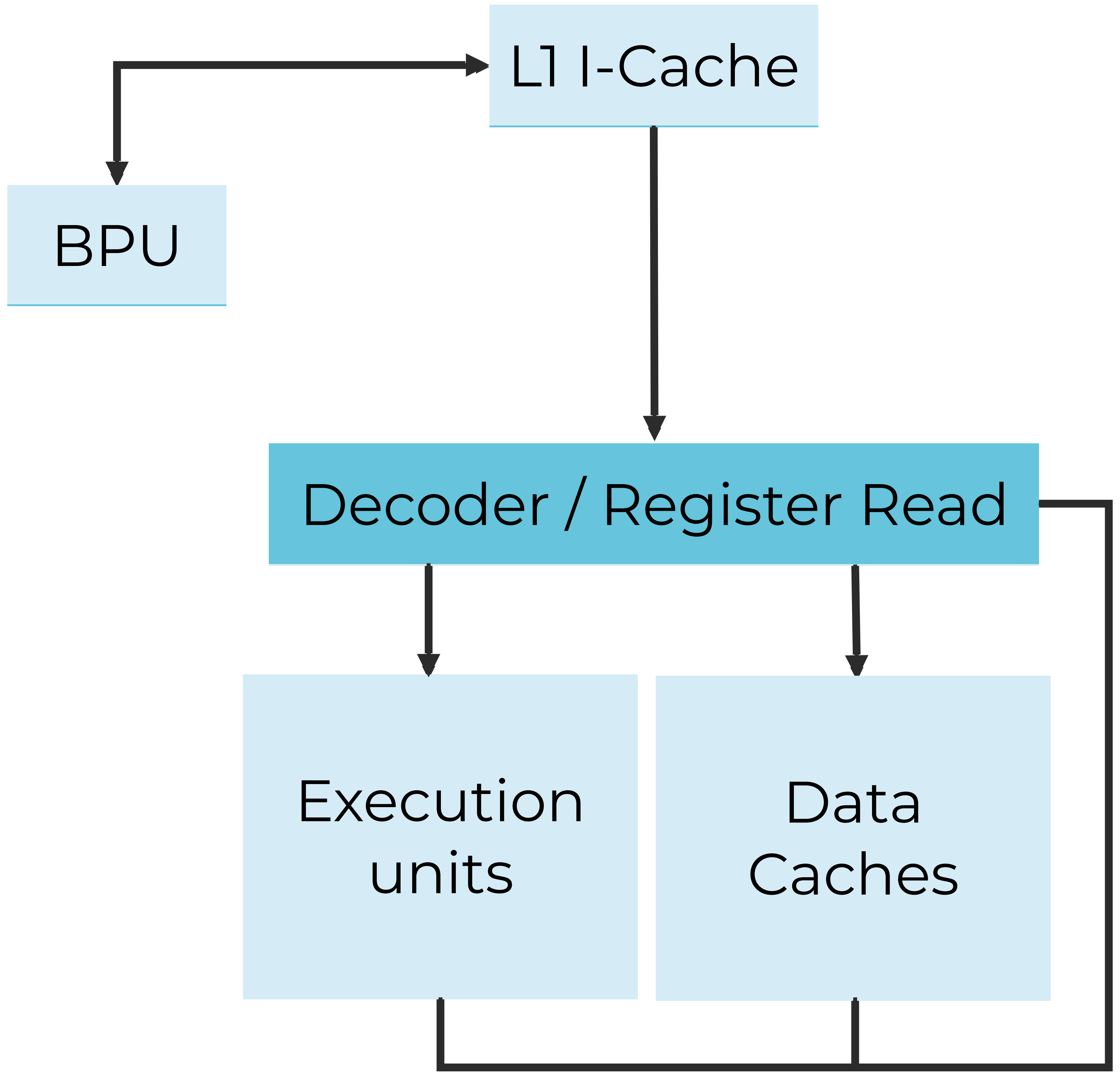
2. Decode instruction and decide what to do



How Does a CPU Work?

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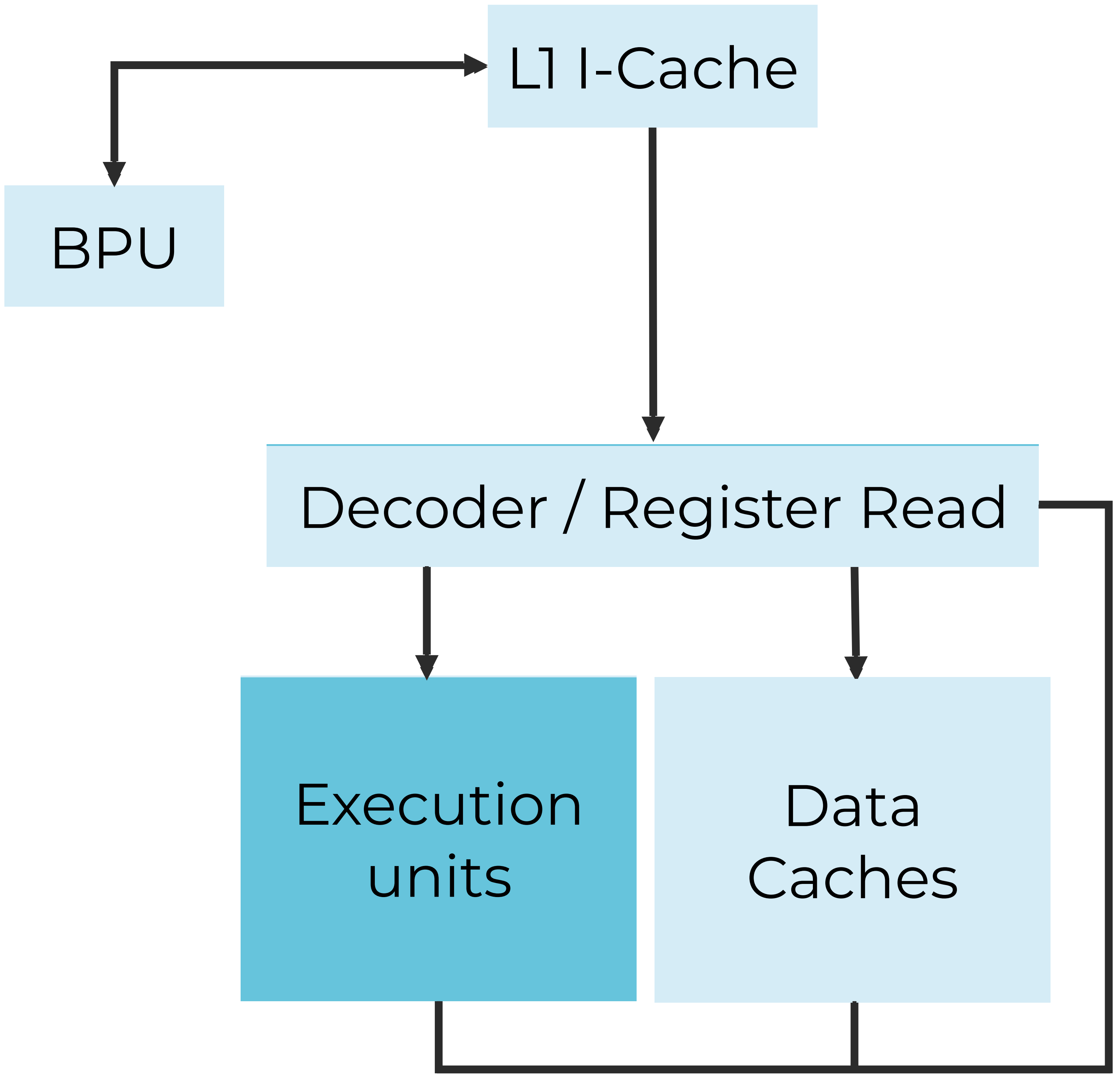

How Does a CPU Work?

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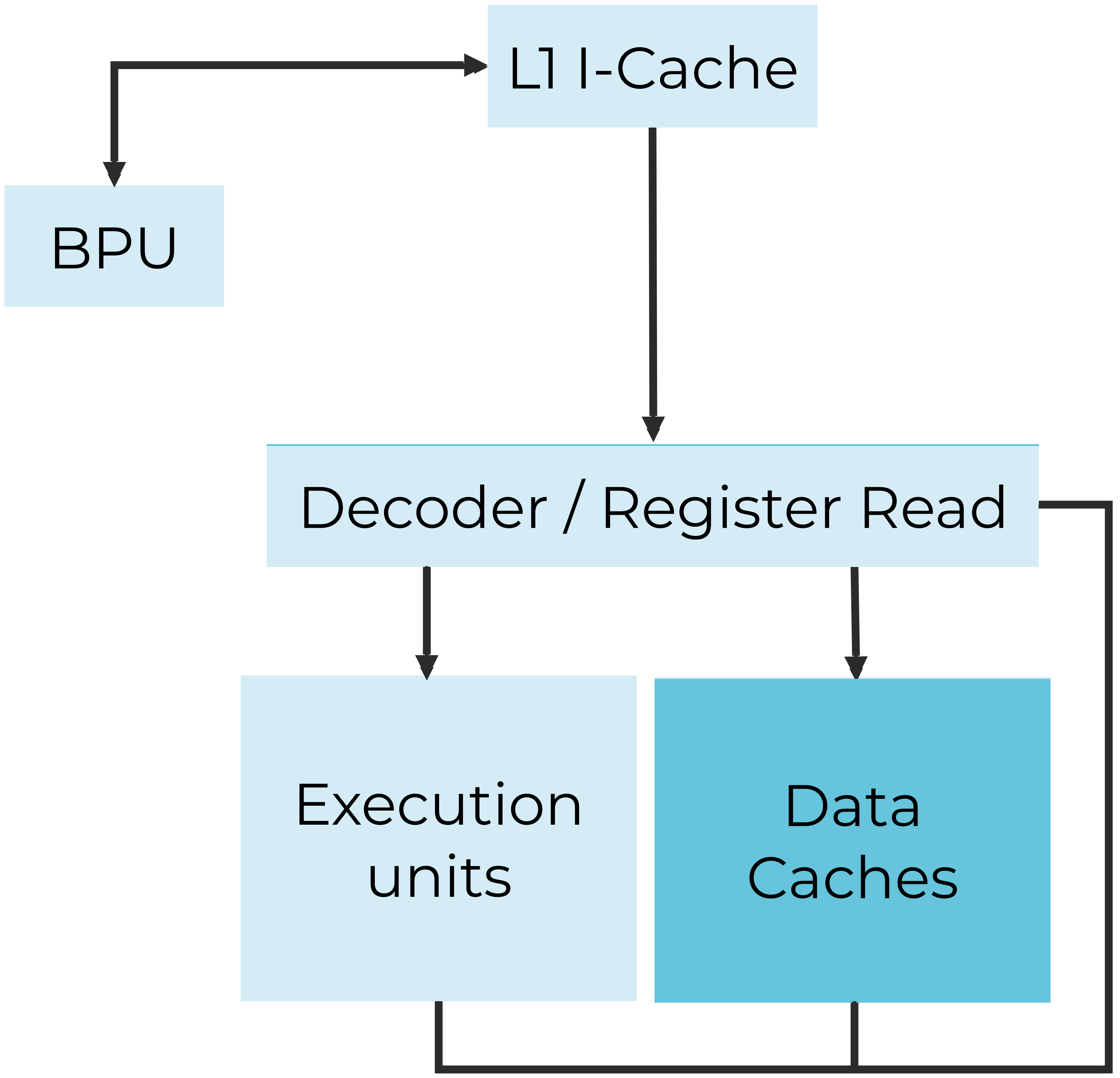
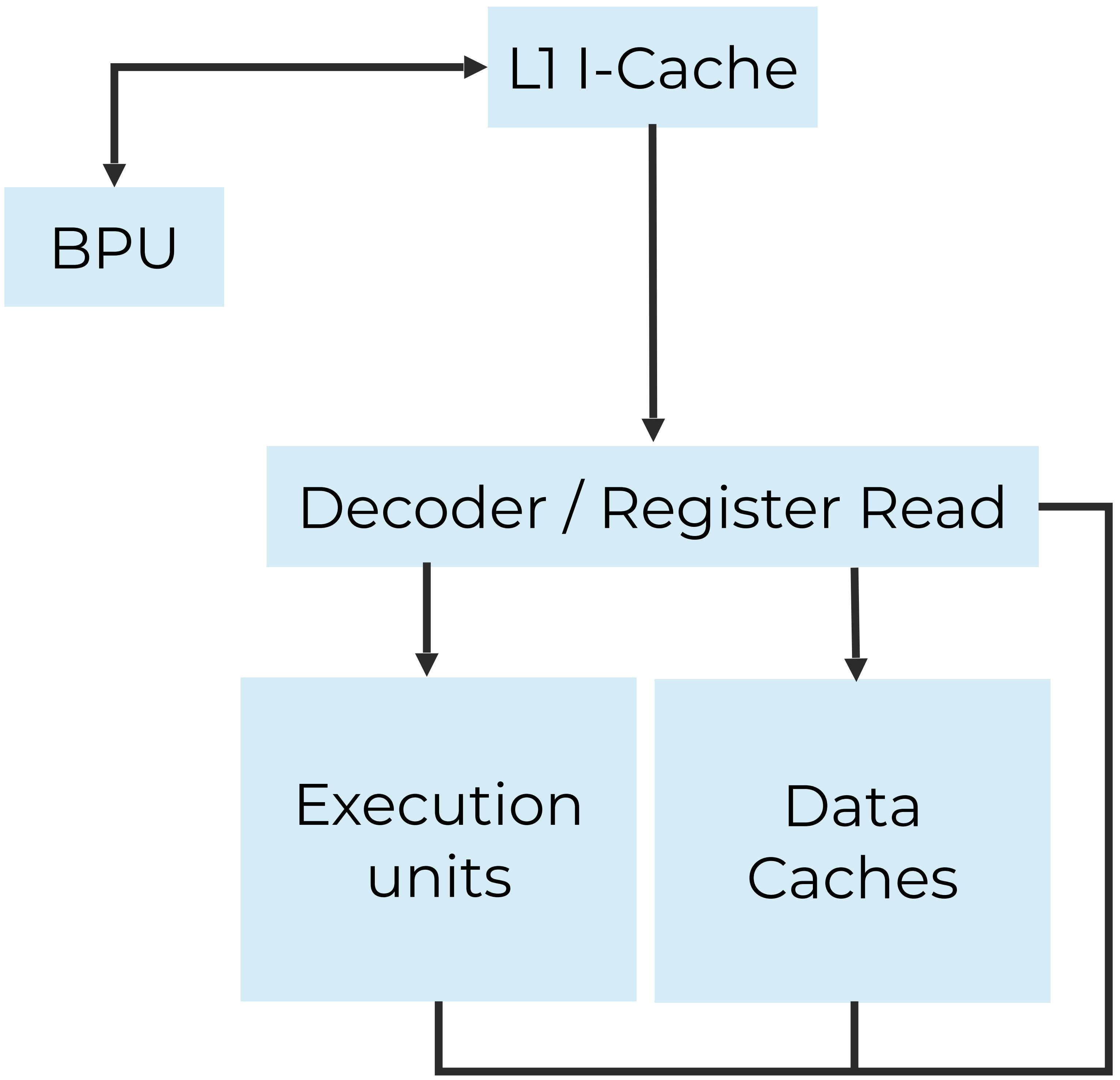
2. Decode instruction and decide what to do
3. Execute the instruction
4. Write back the results to memory



What Type of Attacks are There?



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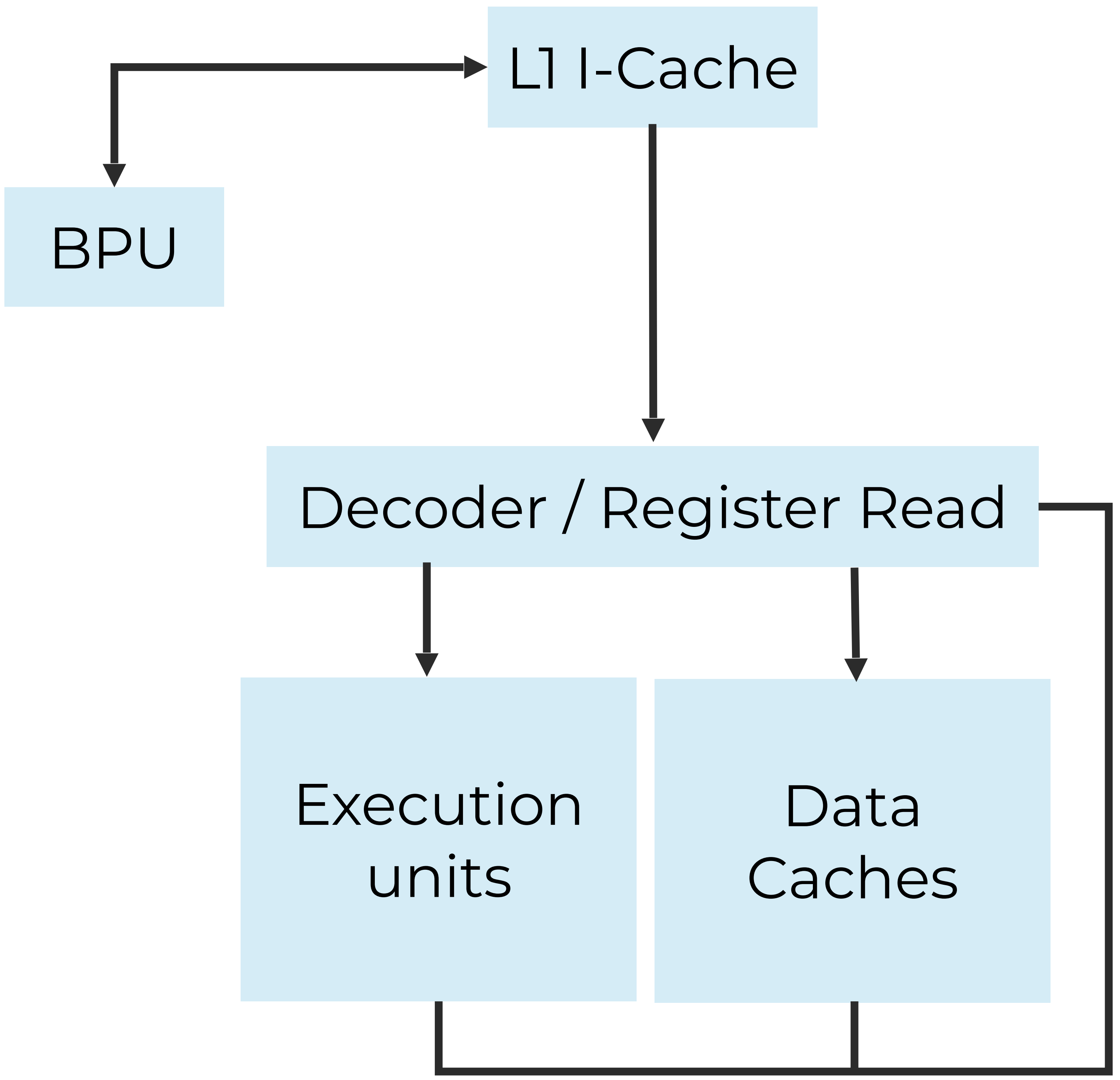
- Attack **timing differences** in caches and predictors



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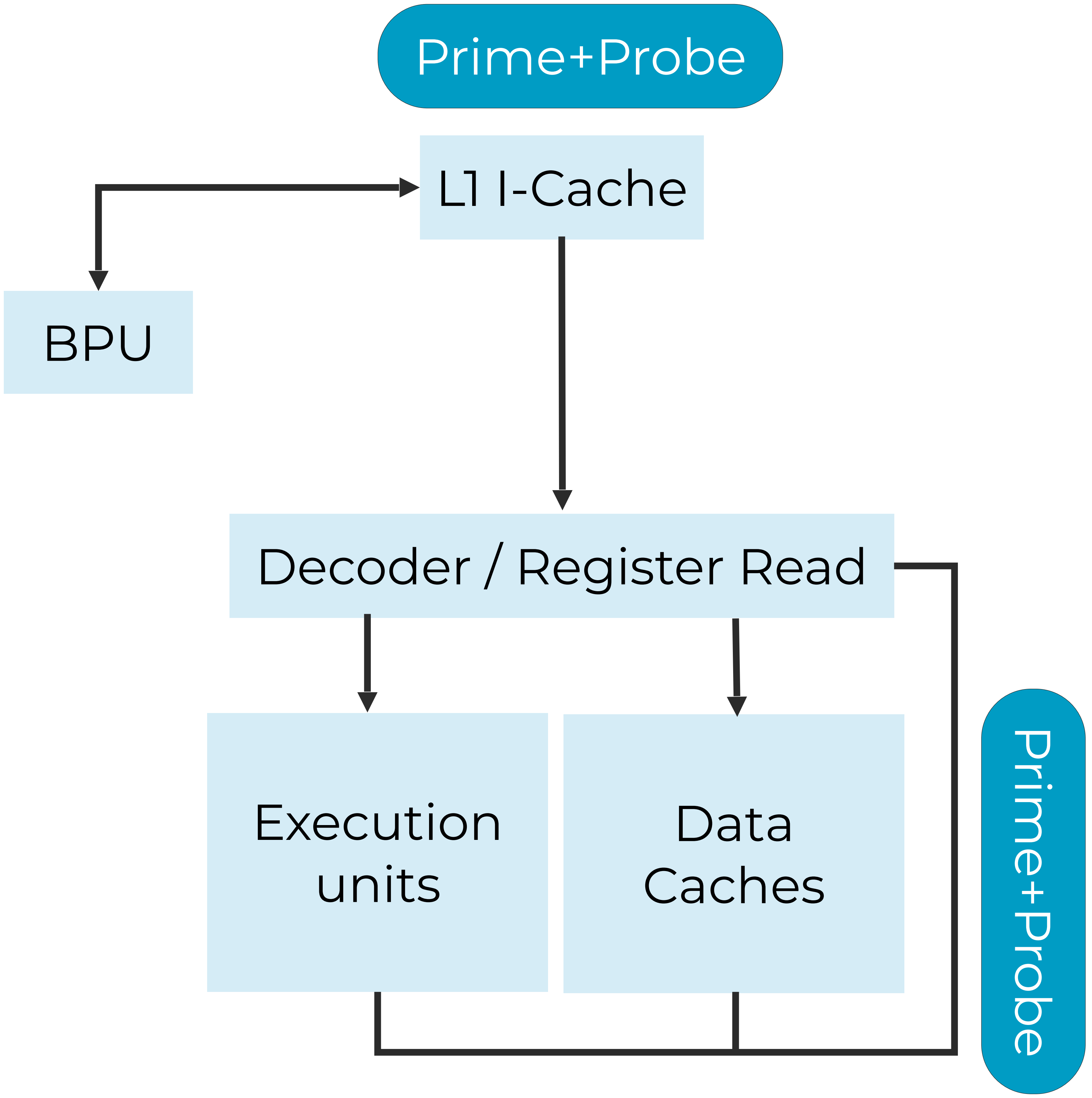

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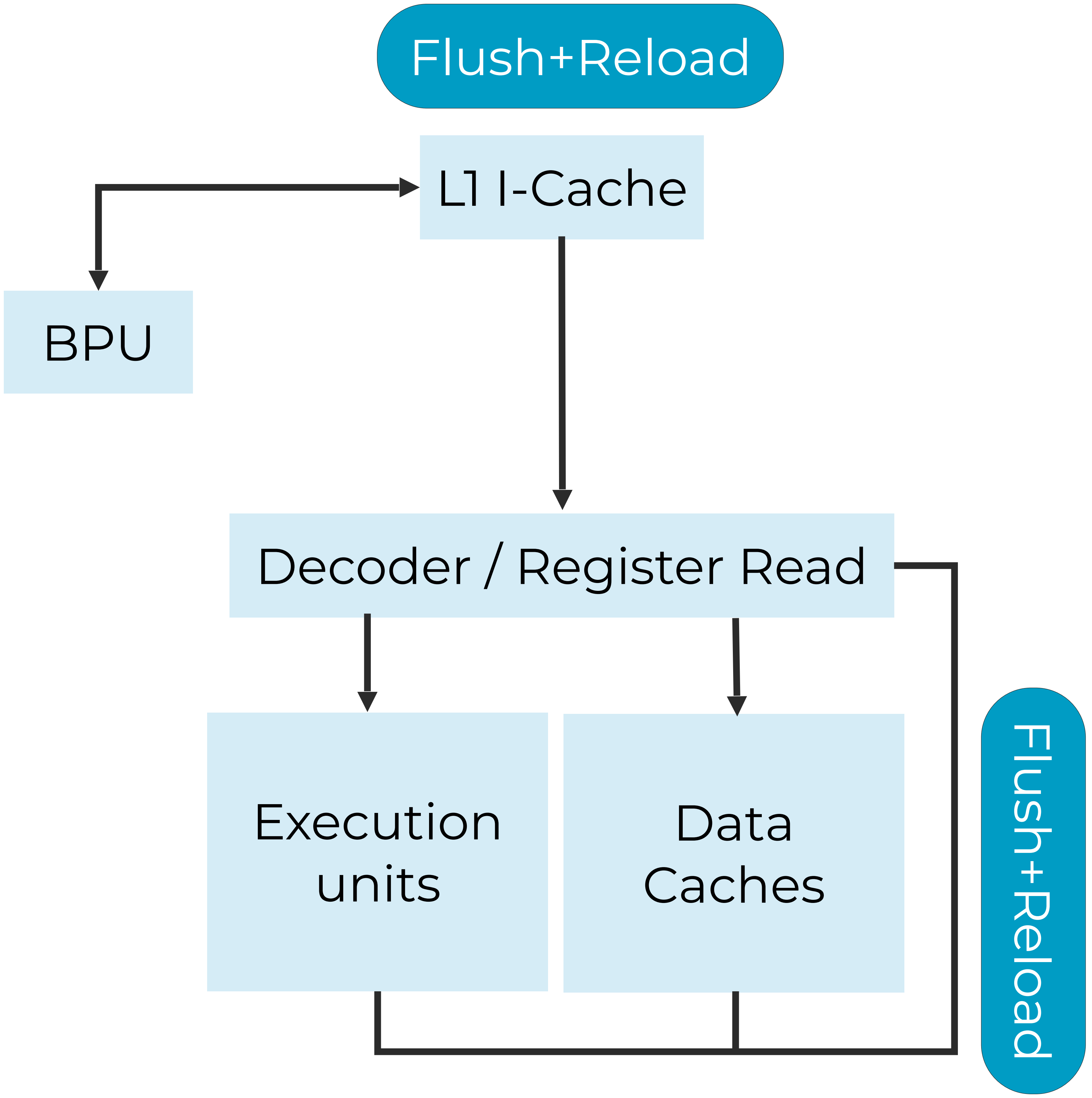

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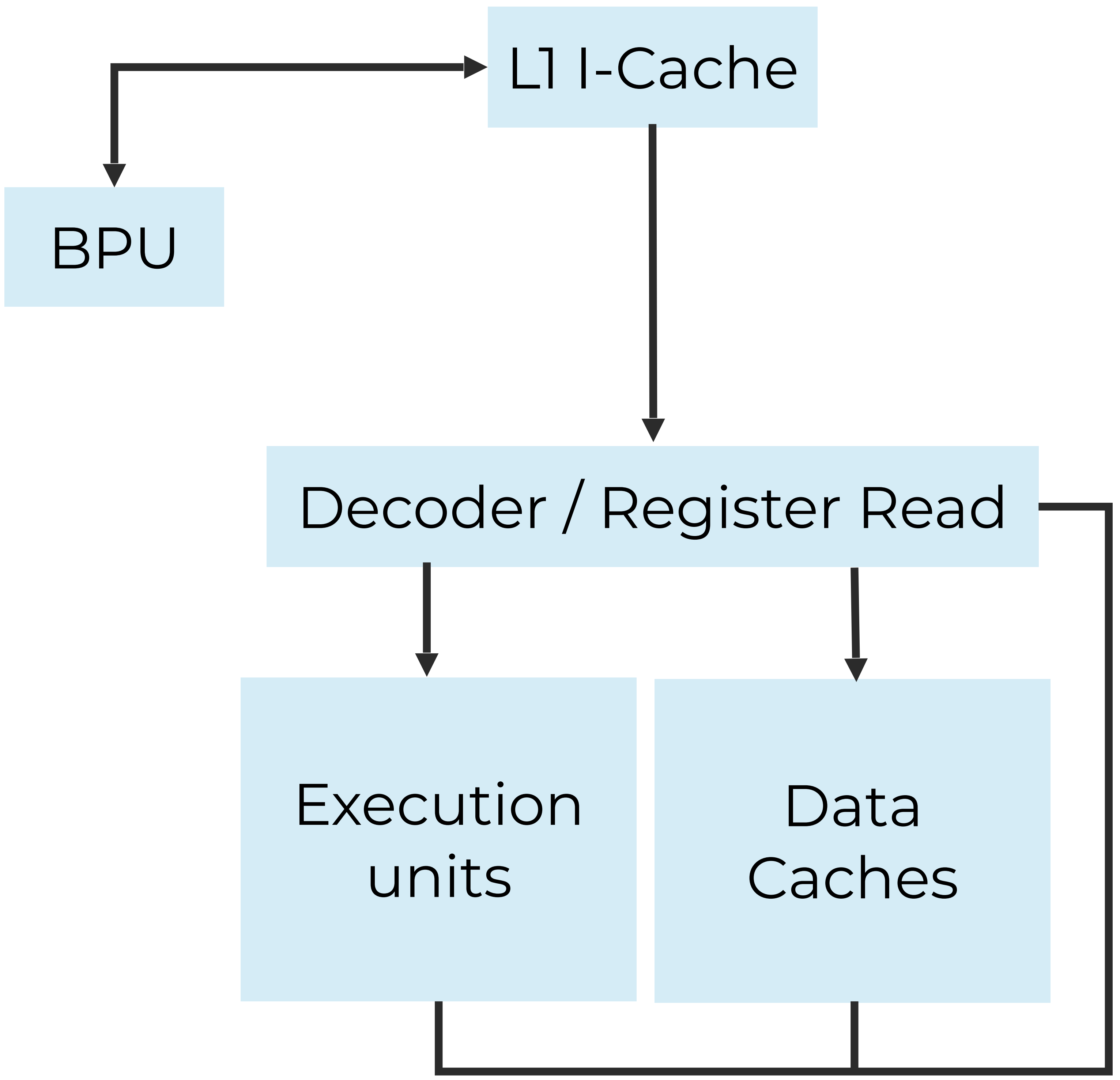
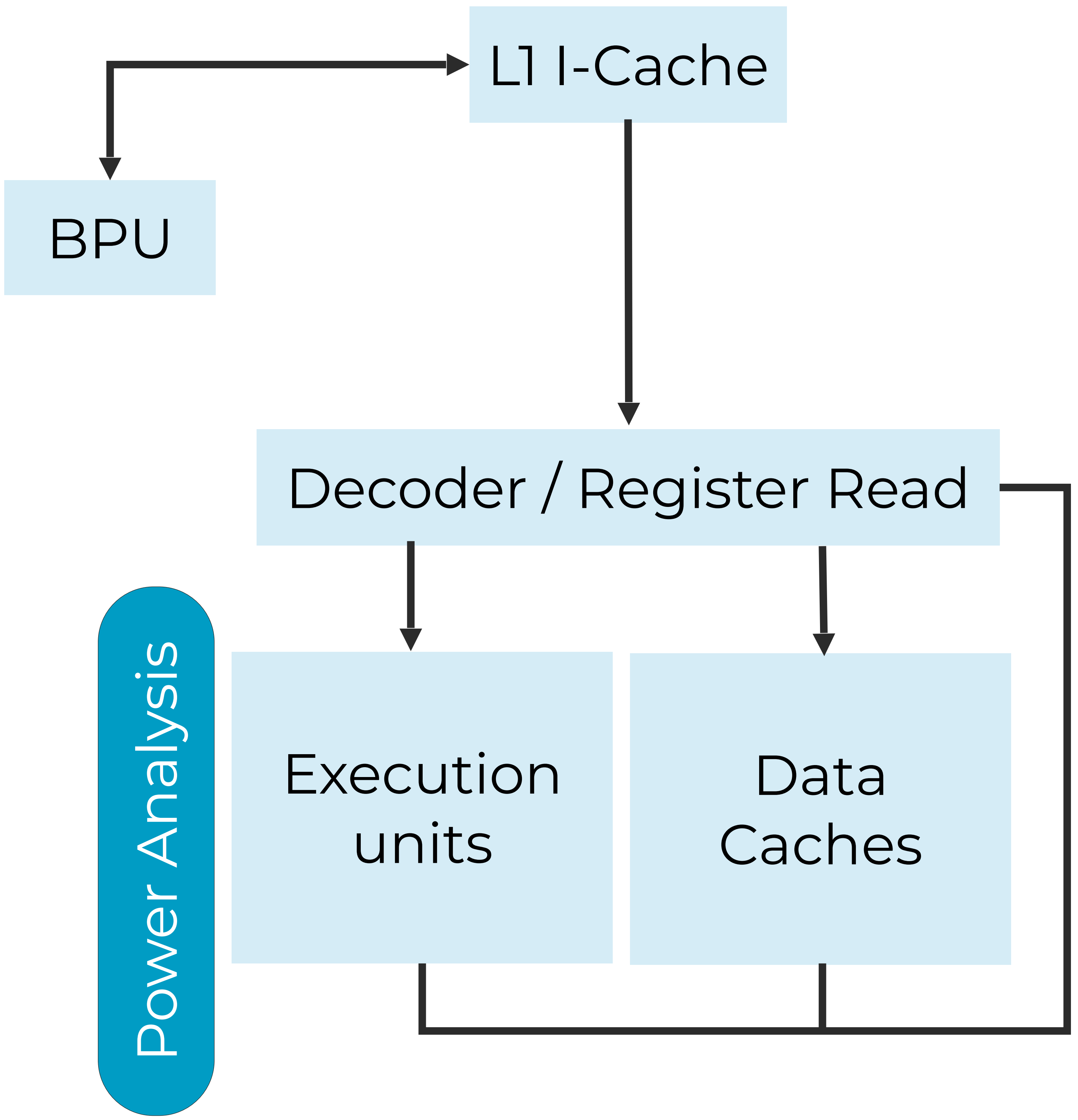
- Exploiting **implementation bugs**



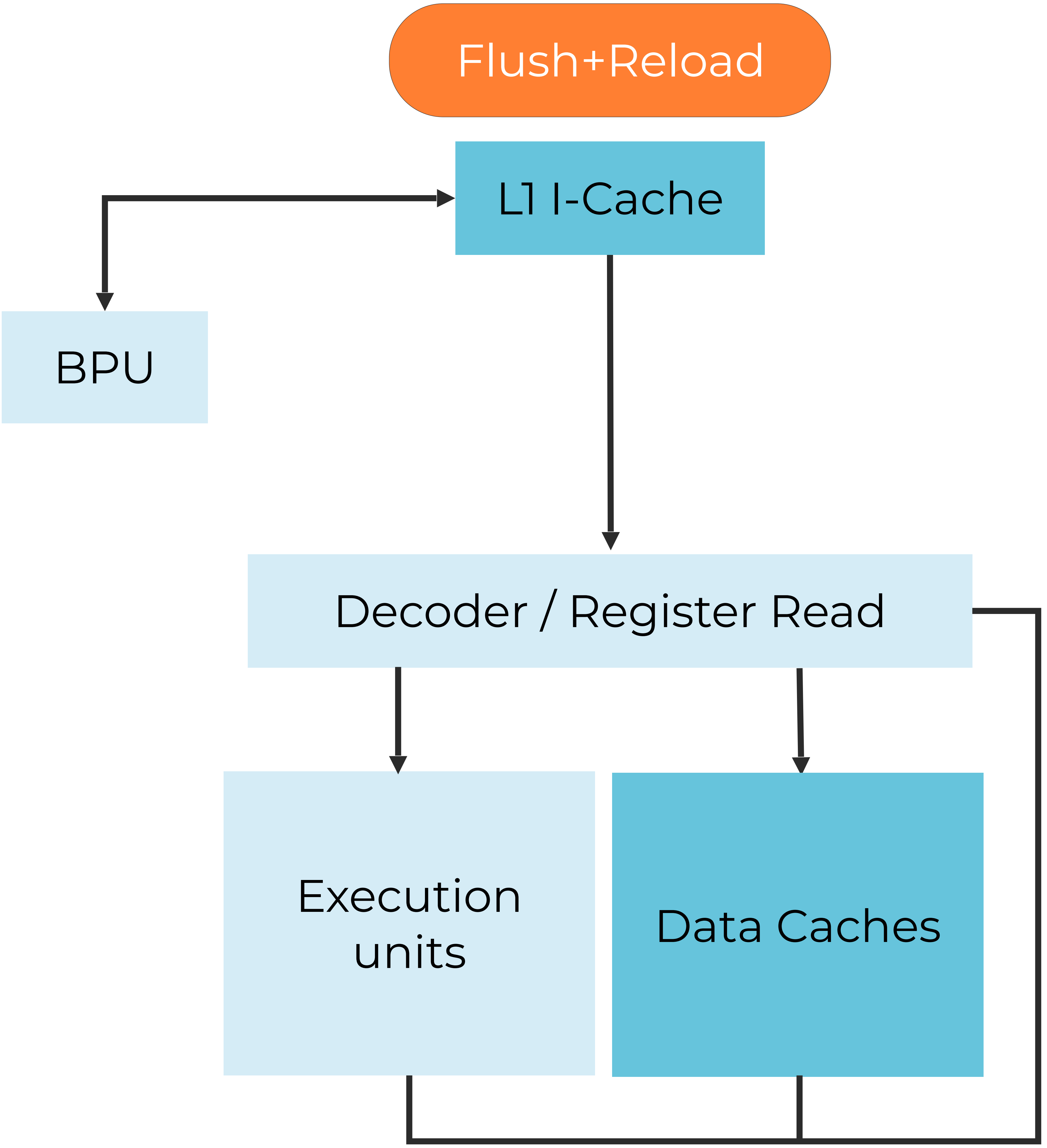
What Type of Attacks are There?

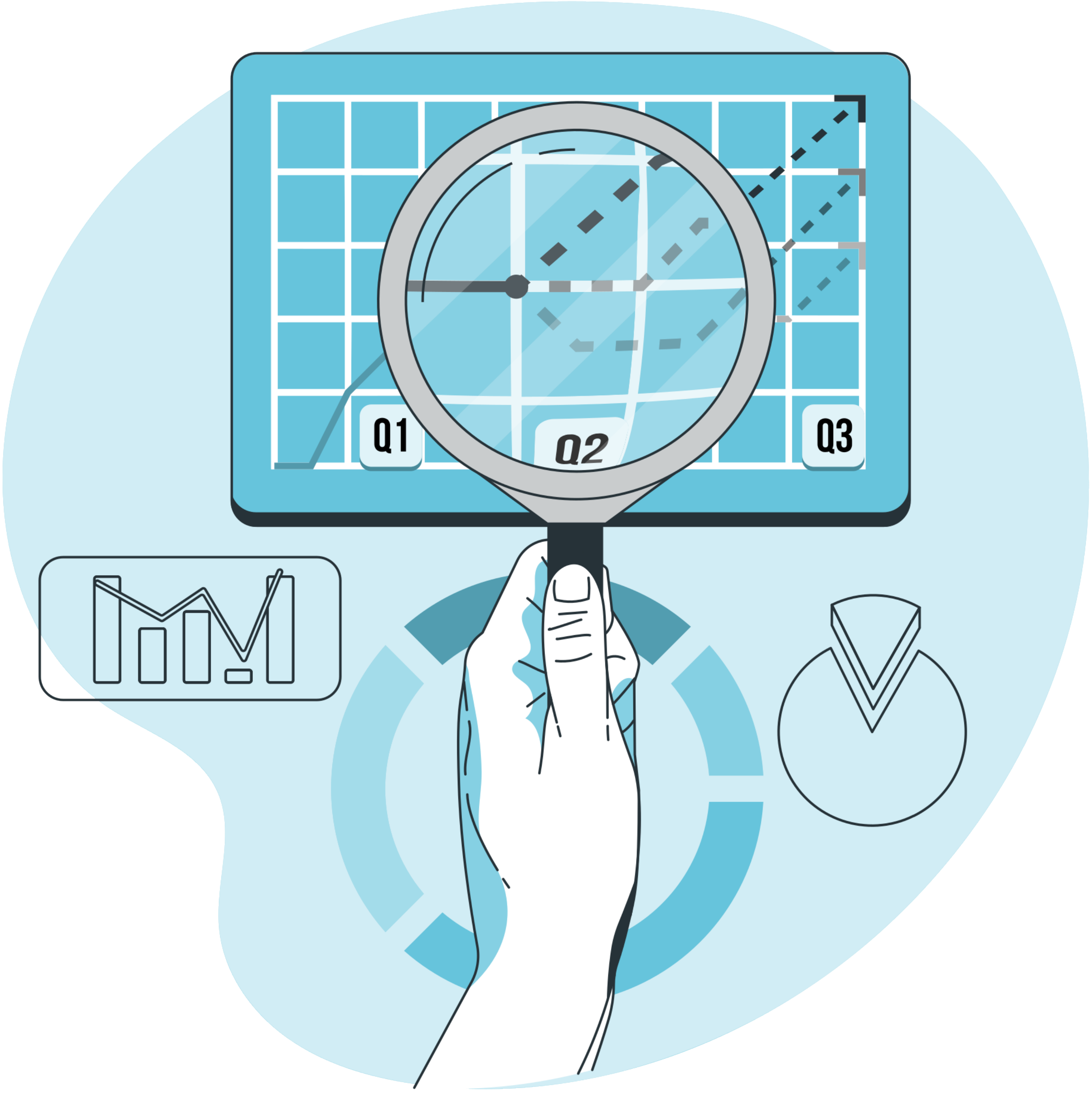
- Attack **timing differences** in caches and predictors
  - Flush+Reload, Prime+Probe
- Exploiting **implementation bugs**
- Abusing **physical properties**
  - Rowhammer
  - Power Analysis



Let’s start with our first attack!

CPU Design: Flush+Reload

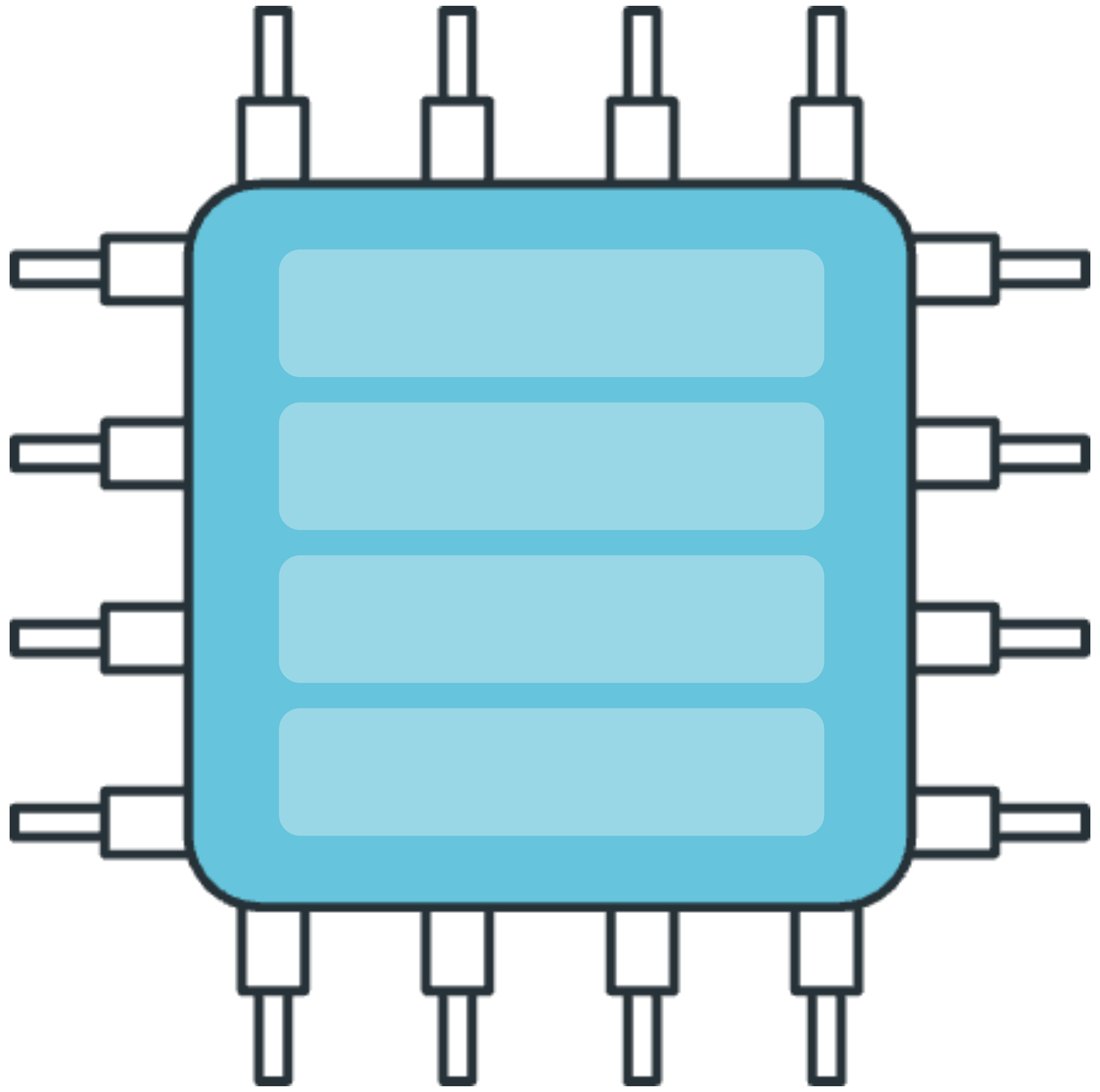




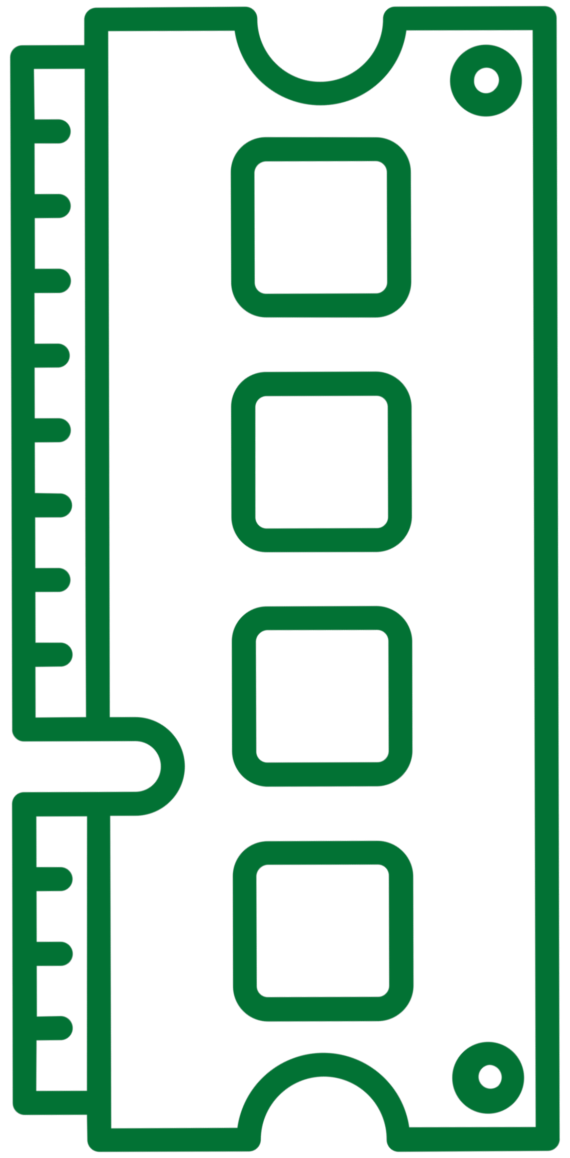
CPU Optimization: The Cache

```
access(array[0]);

access(array[0]);
```



CPU Cache



DRAM

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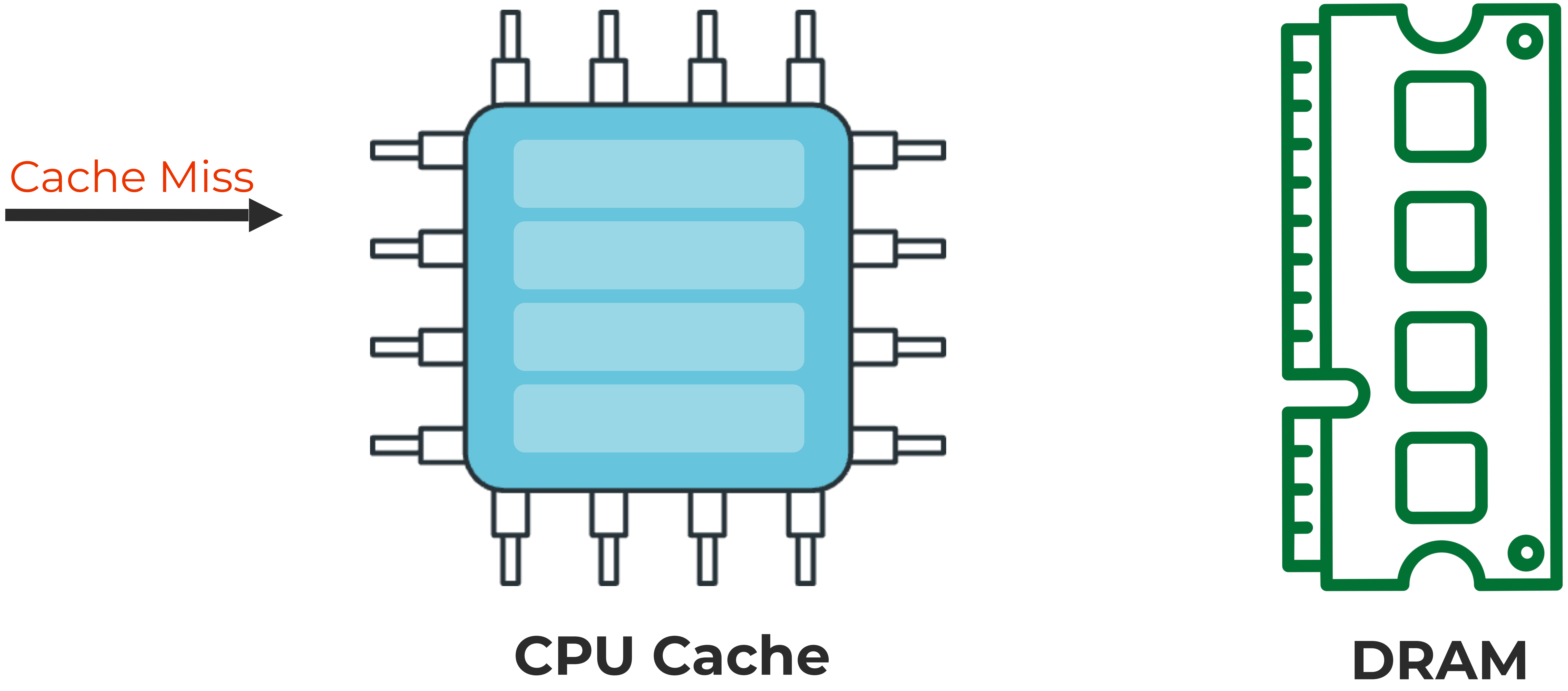

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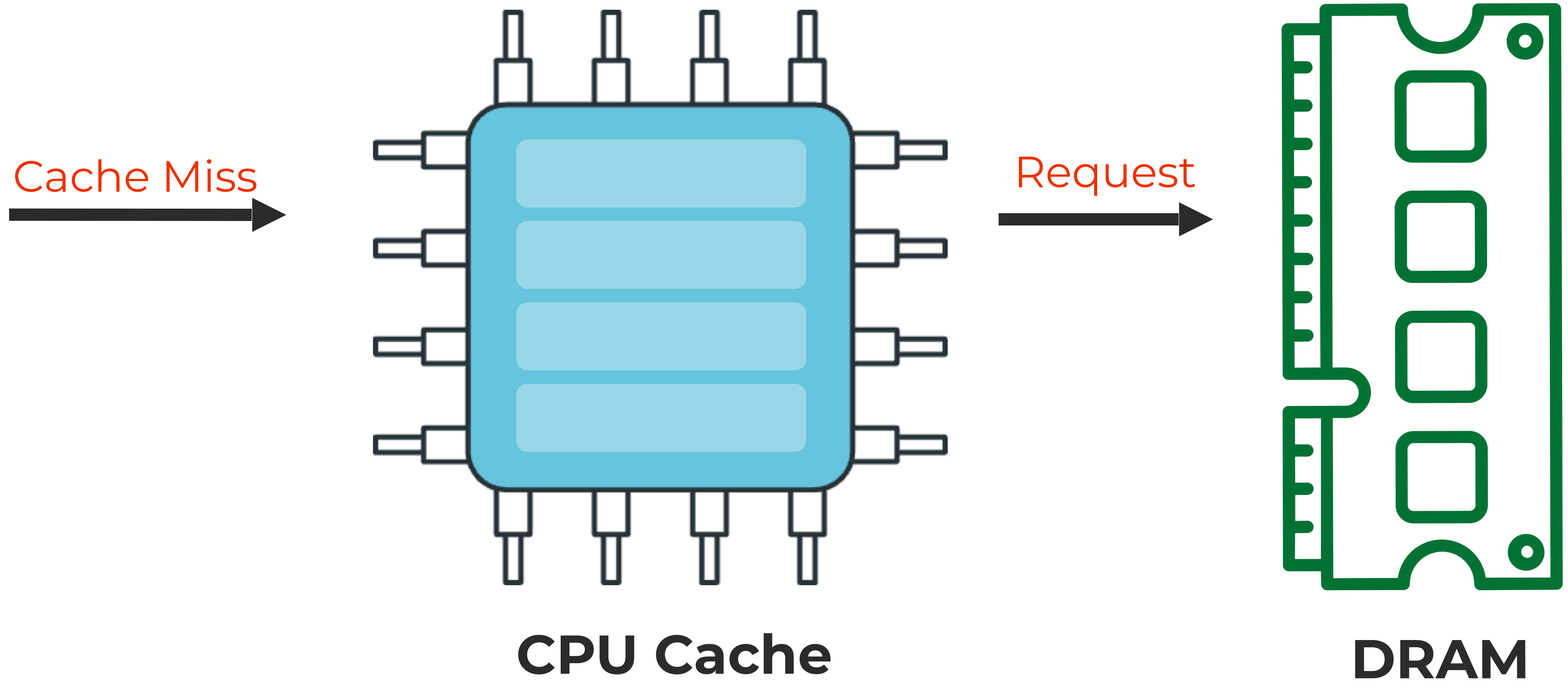

Cache Miss

Request

CPU Cache

DRAM

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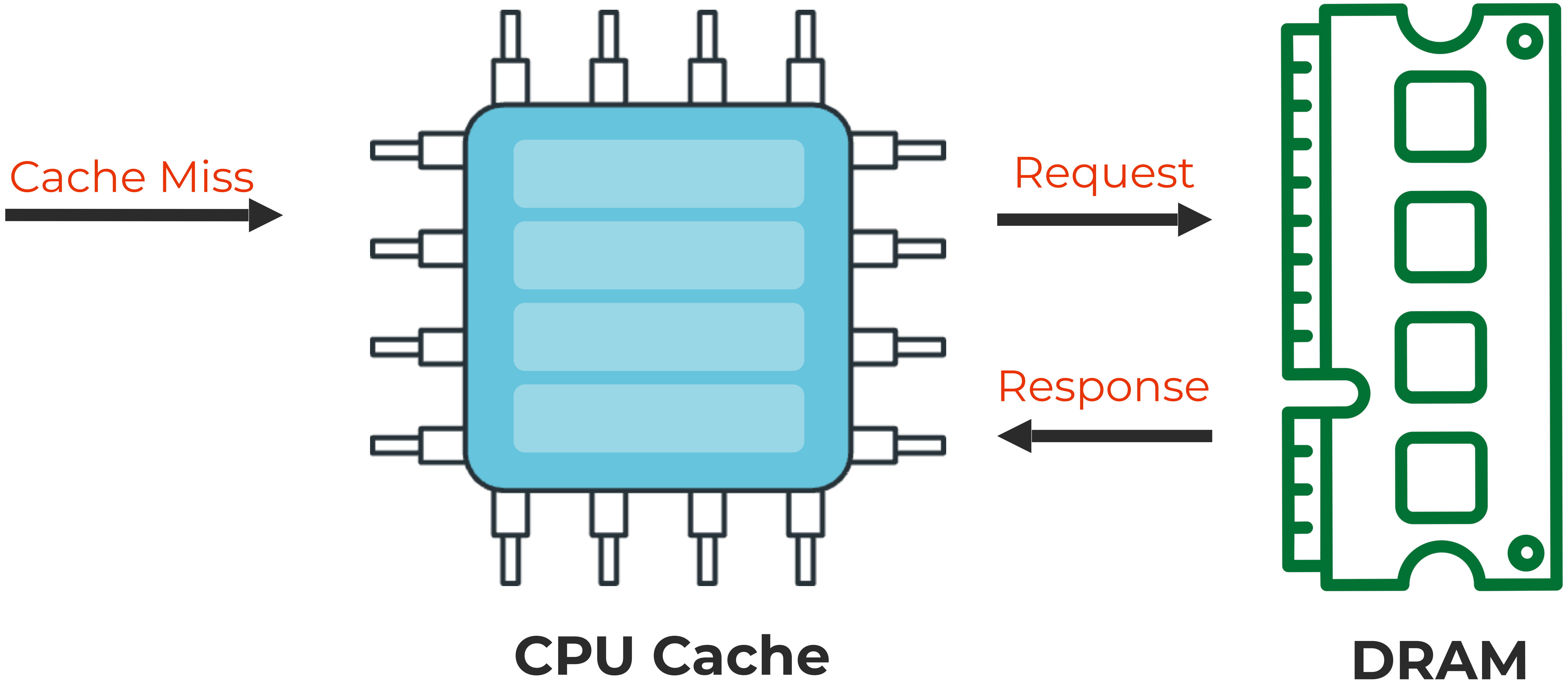

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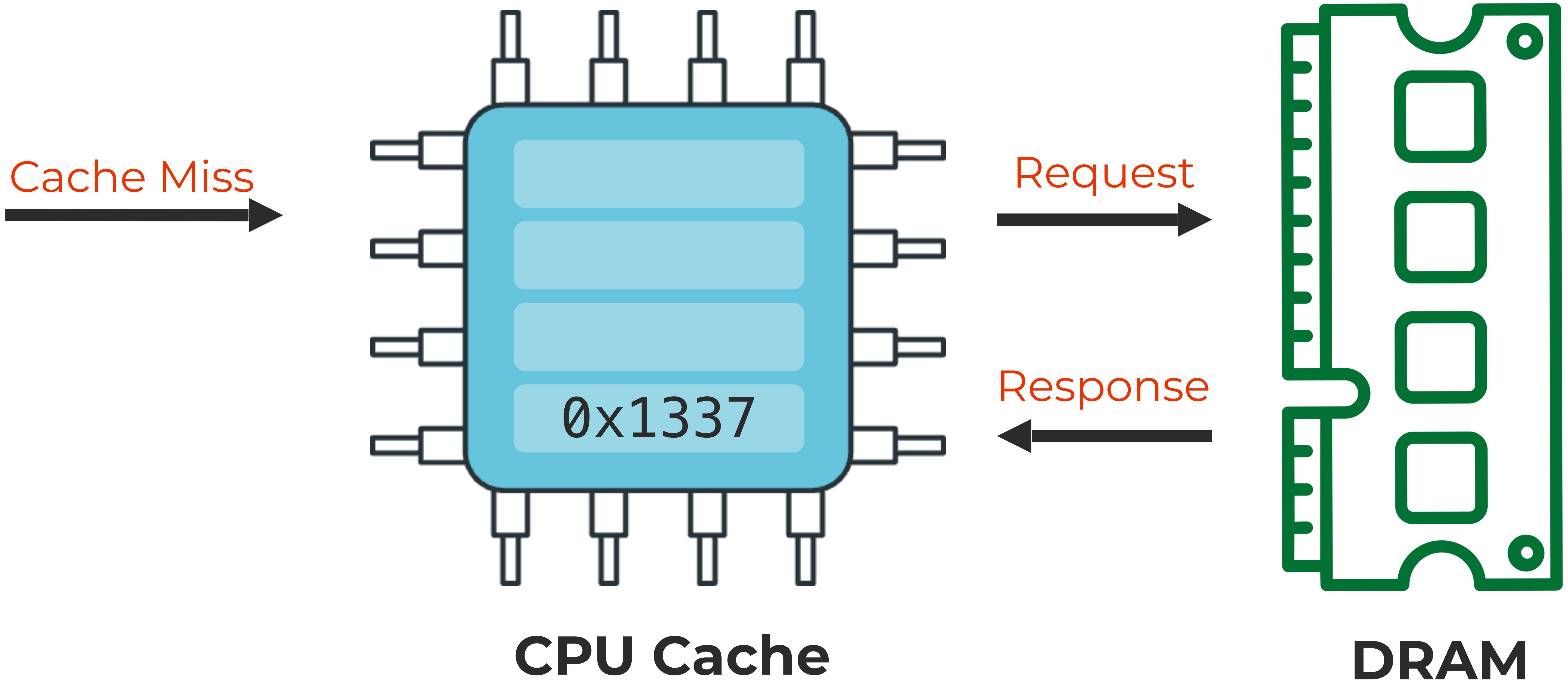

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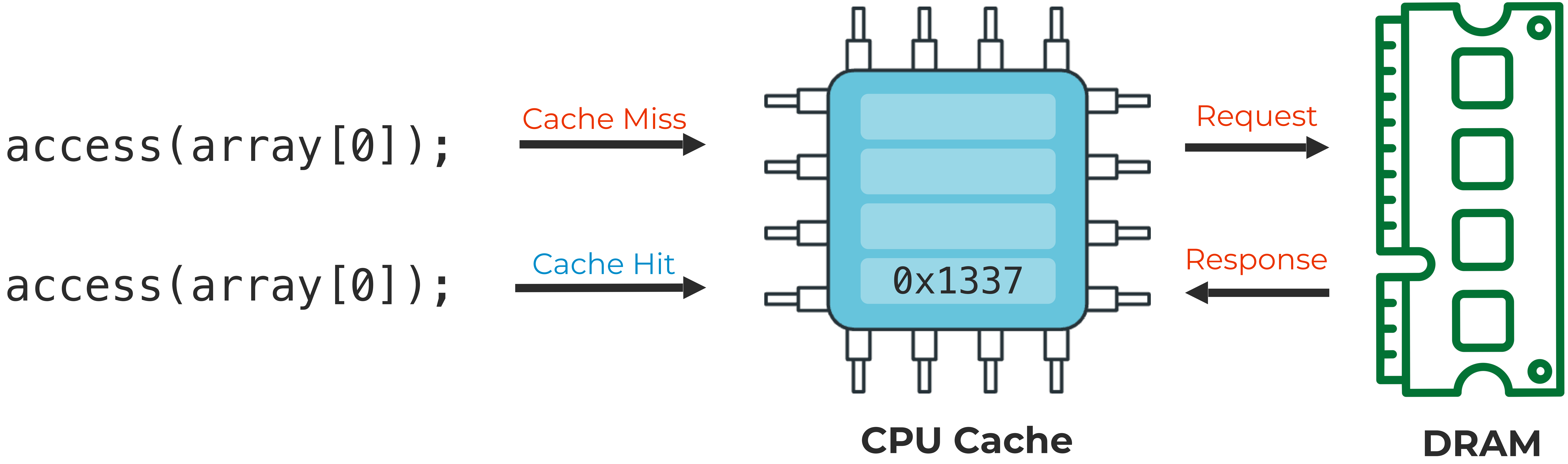

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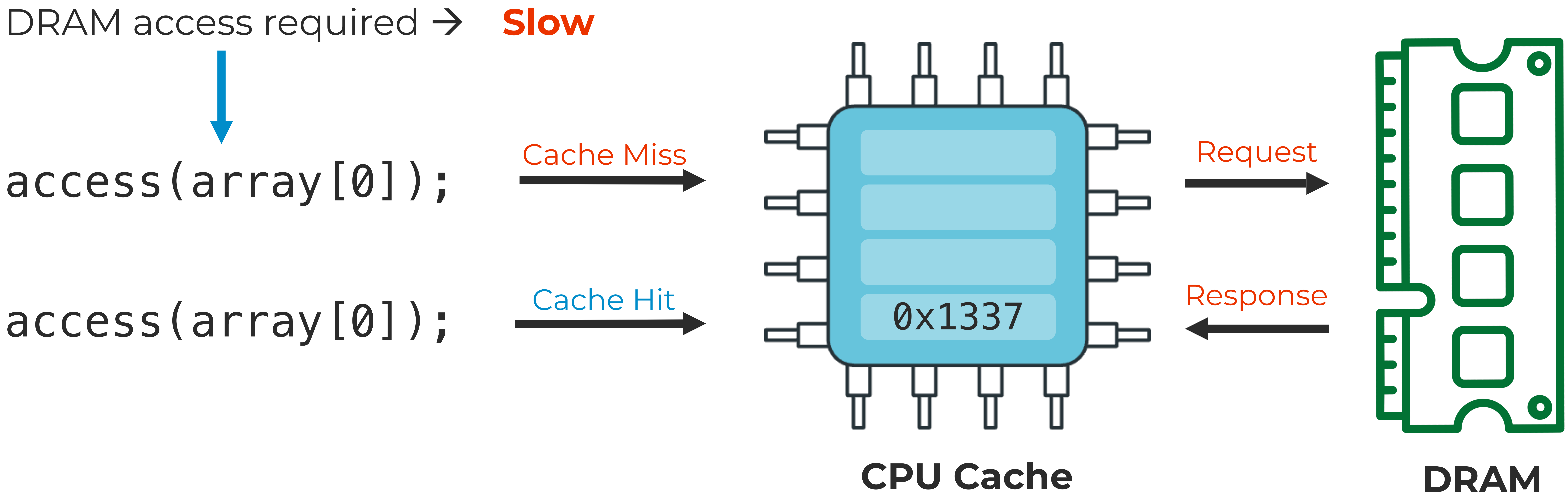

DRAM access required → **Slow**

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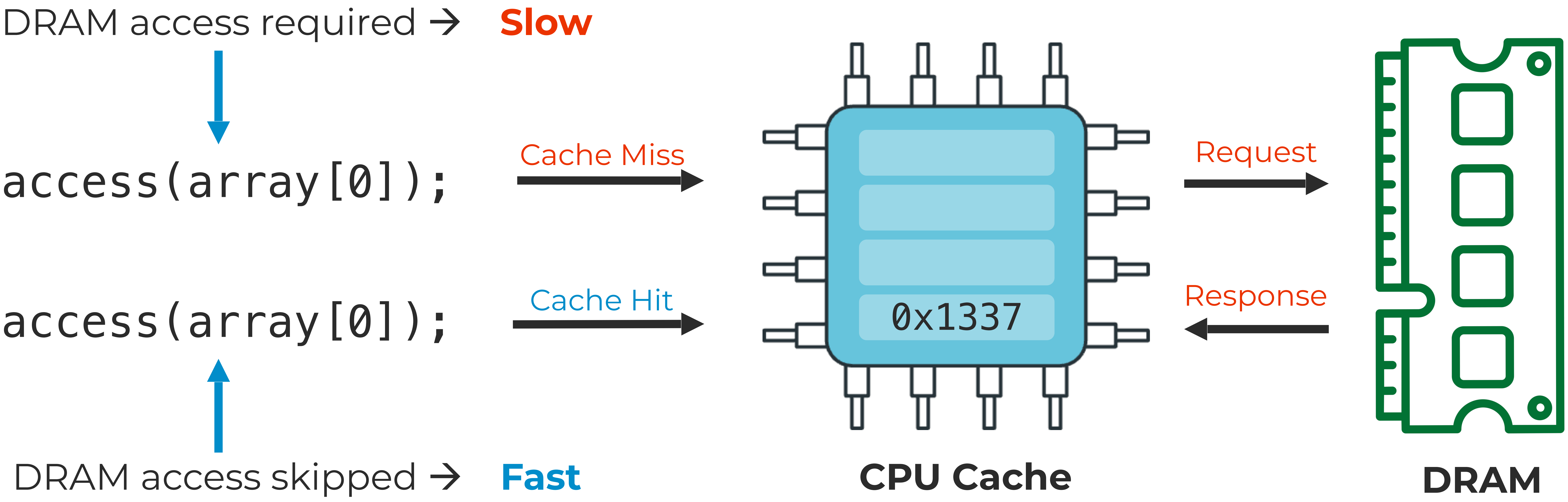

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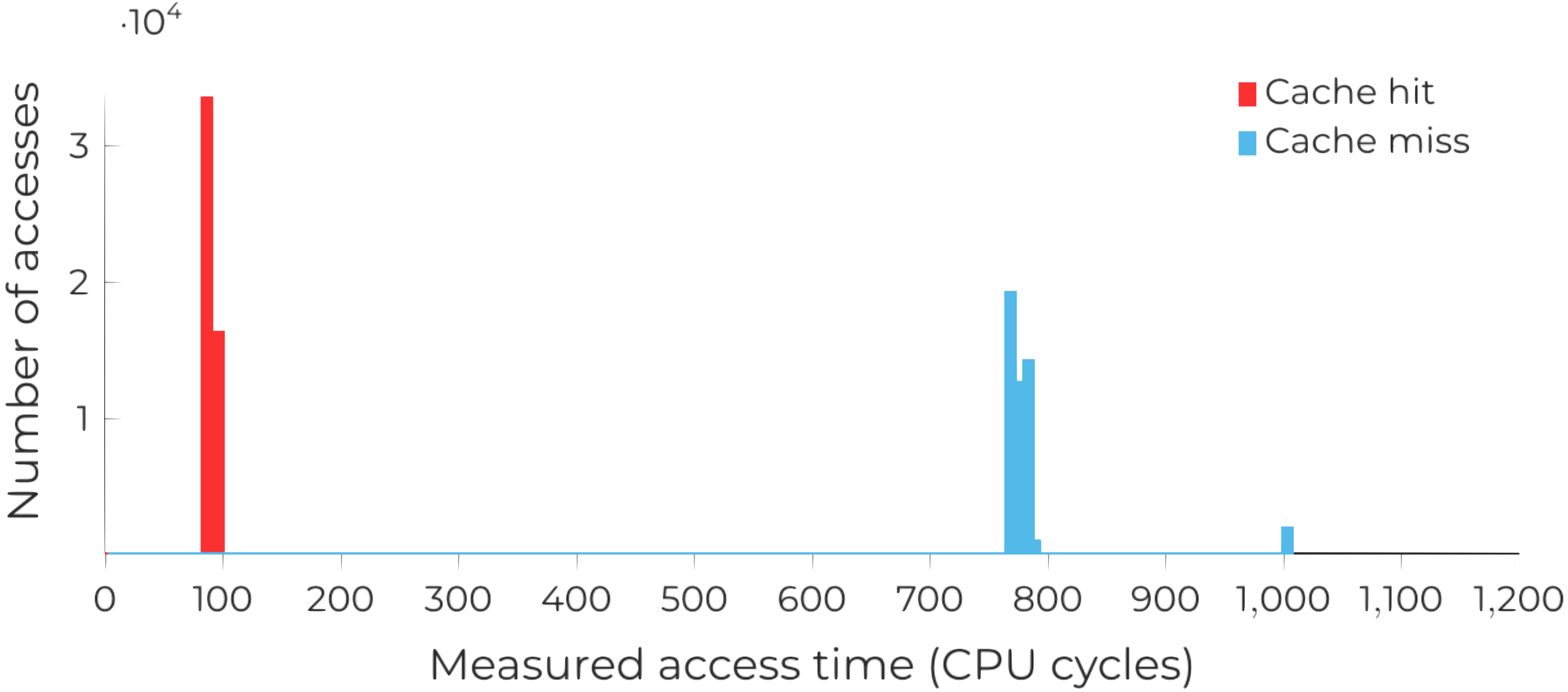
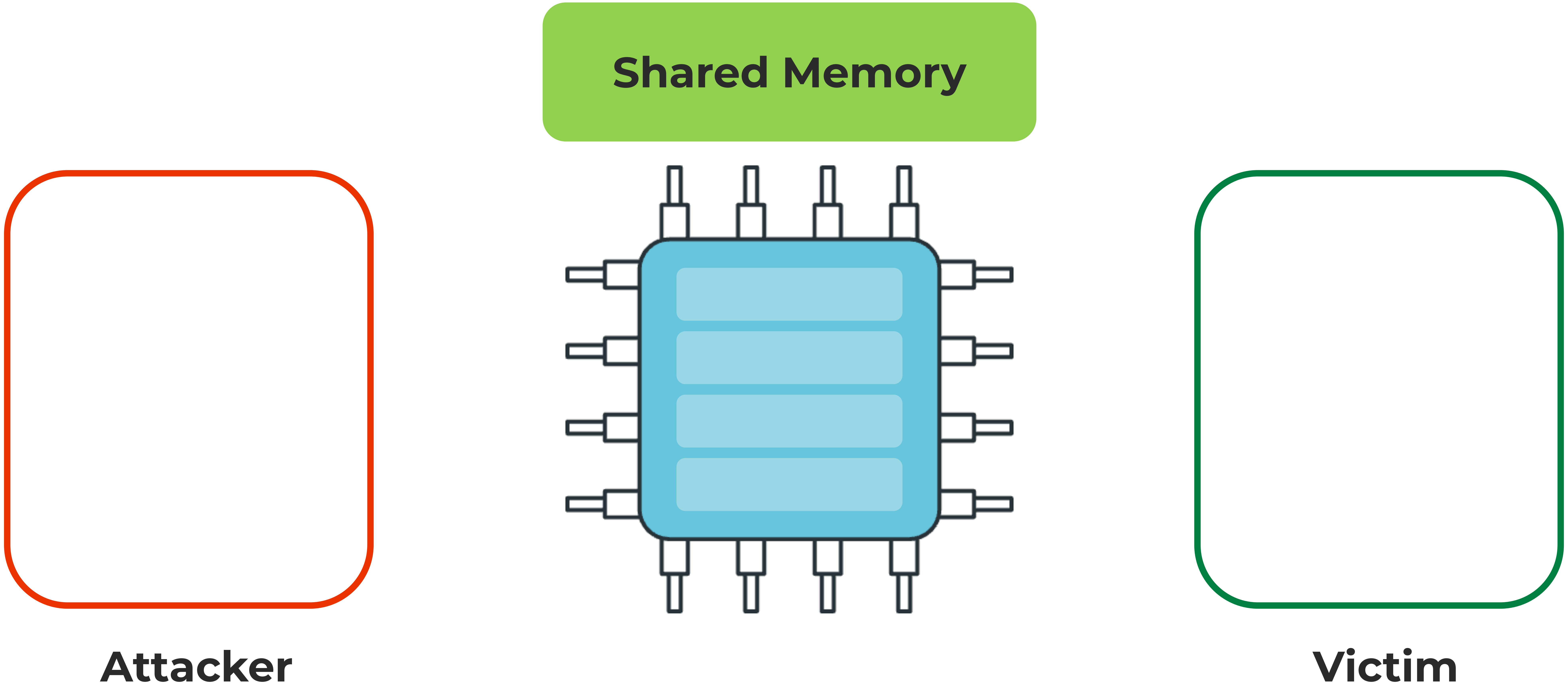
DRAM access skipped → **Fast**

Measuring Cache Timings



Flush+Reload: Shared Memory



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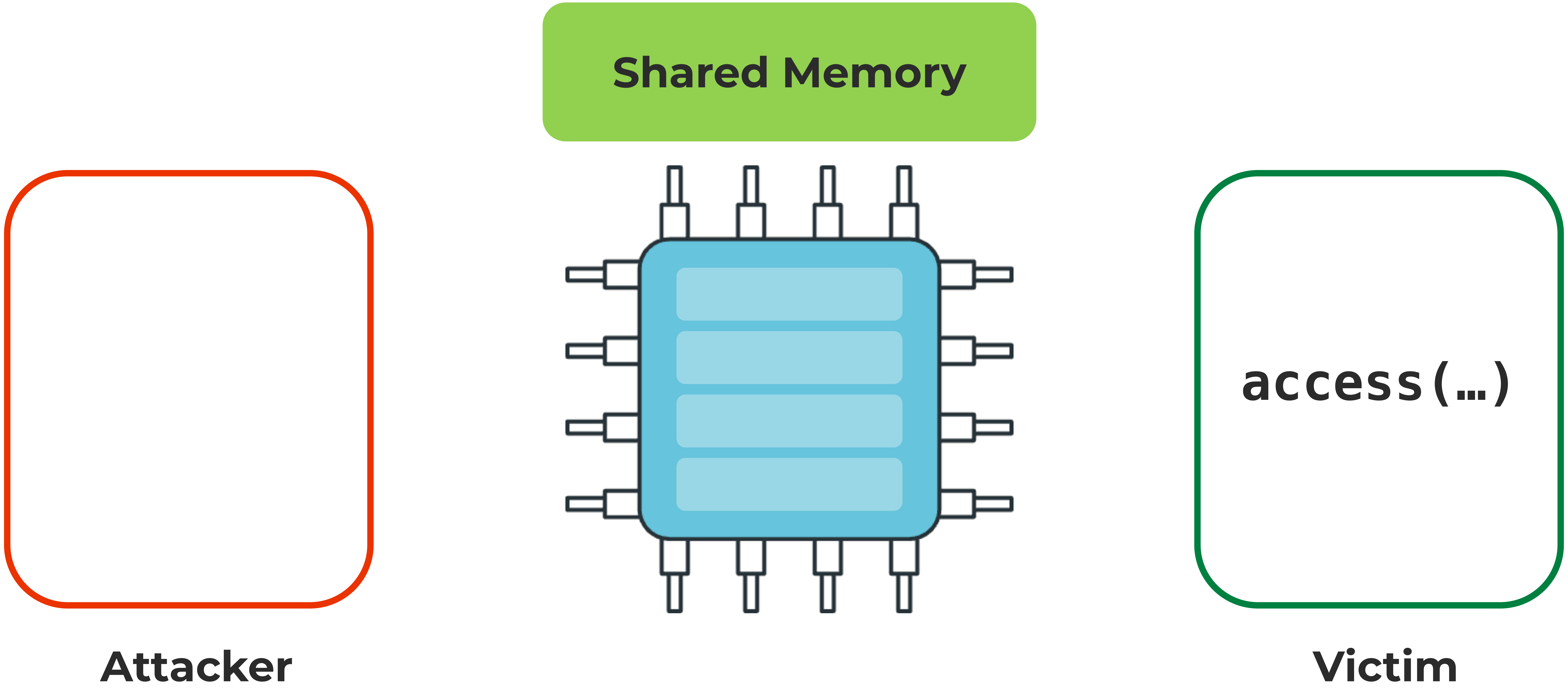

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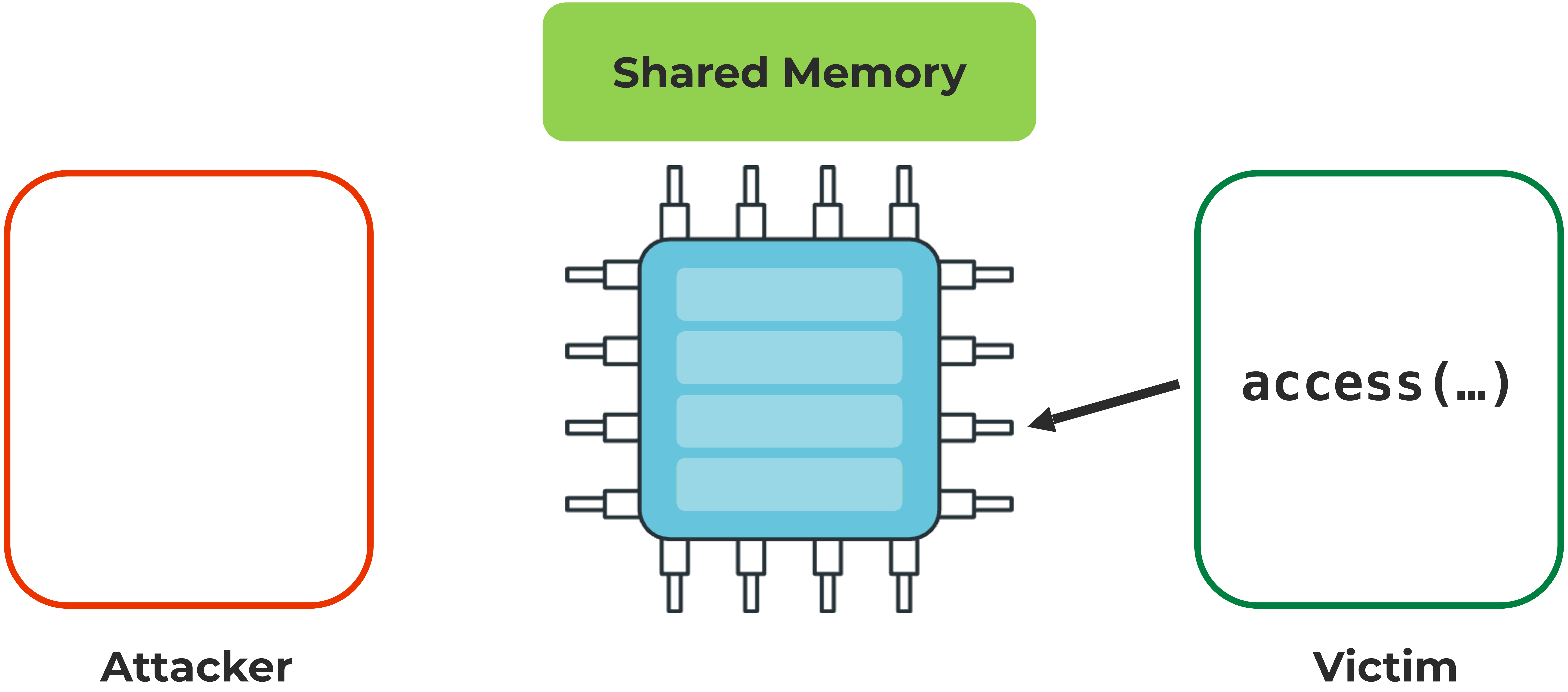

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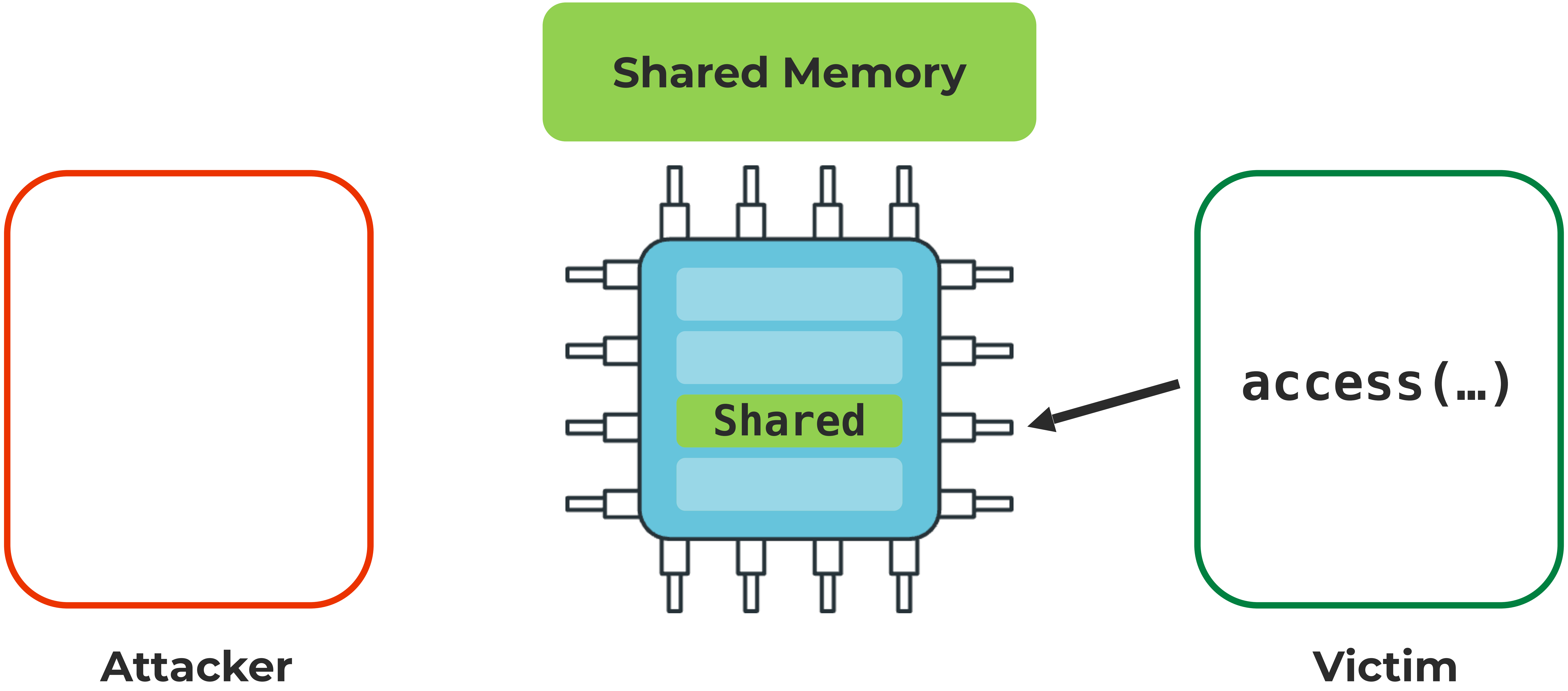

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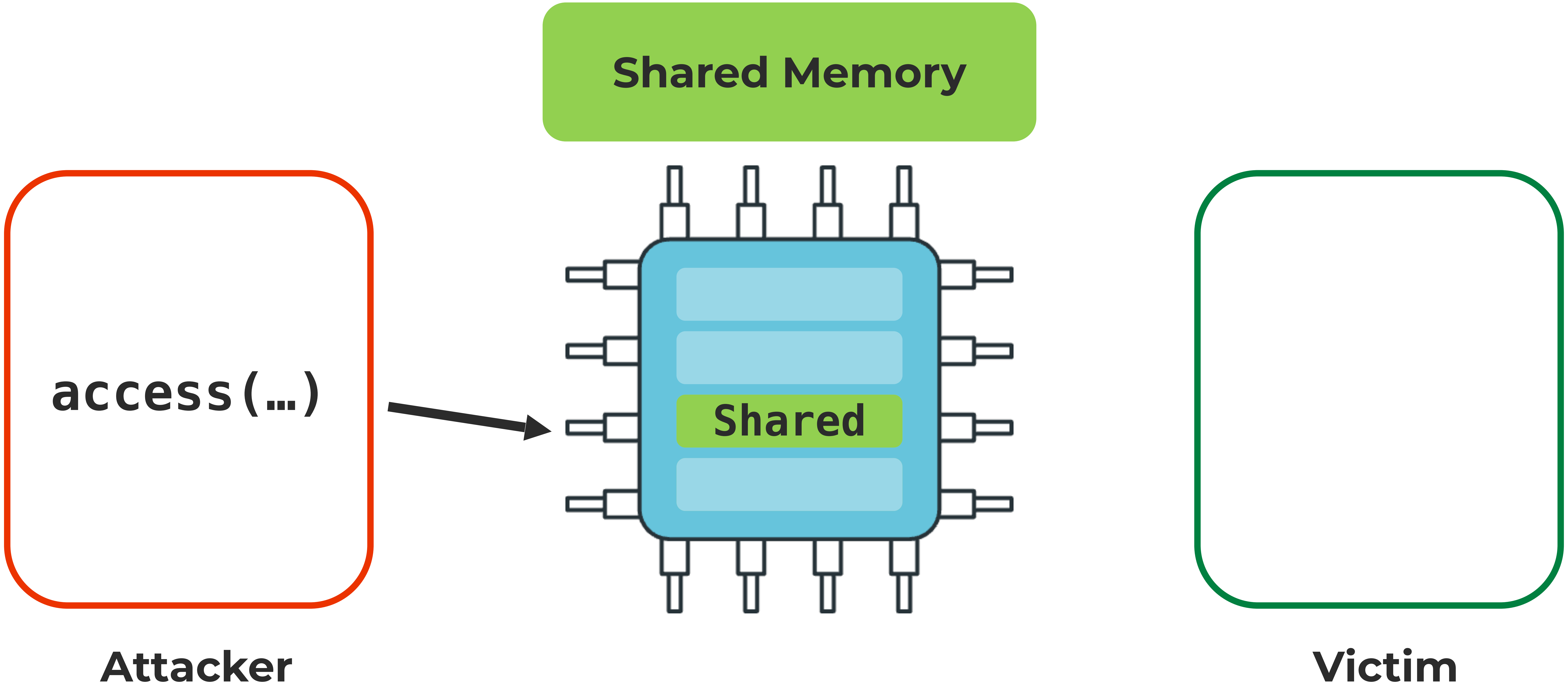

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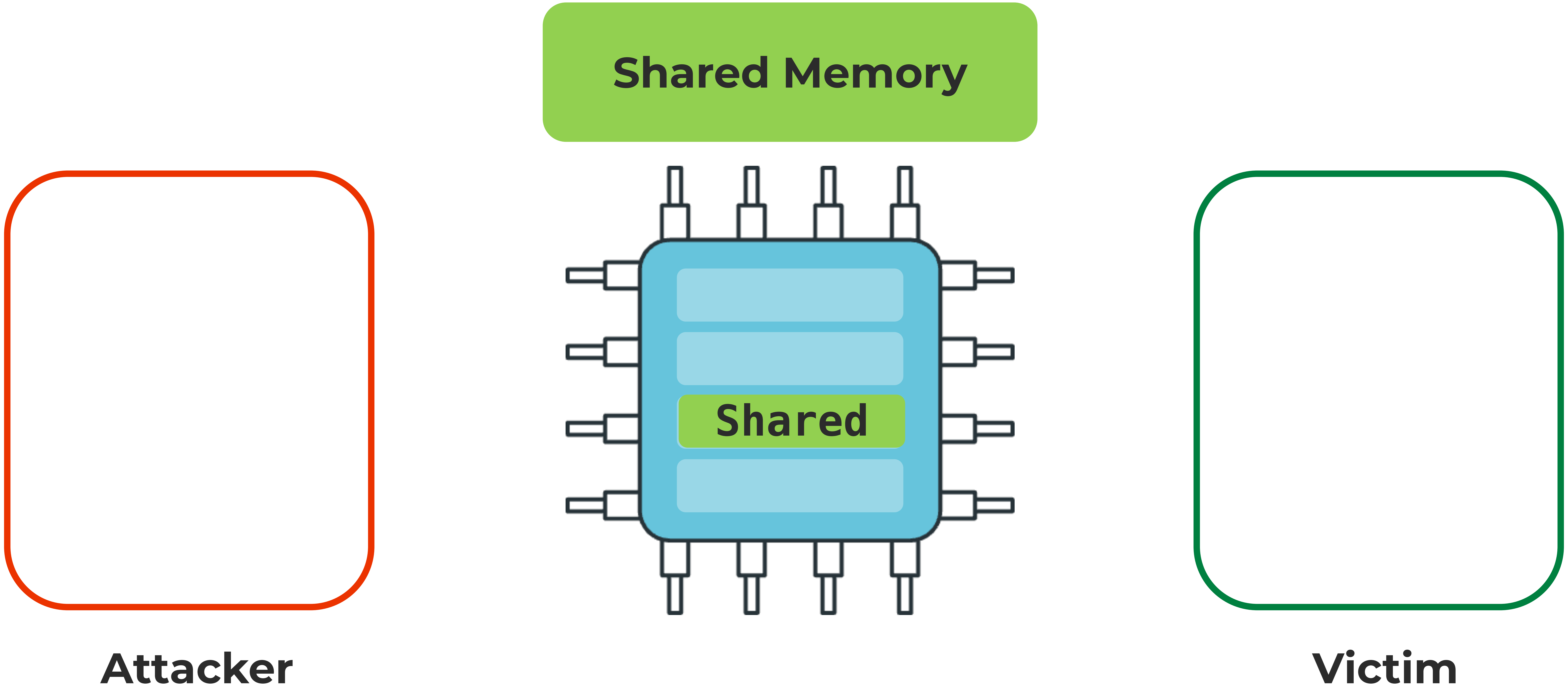

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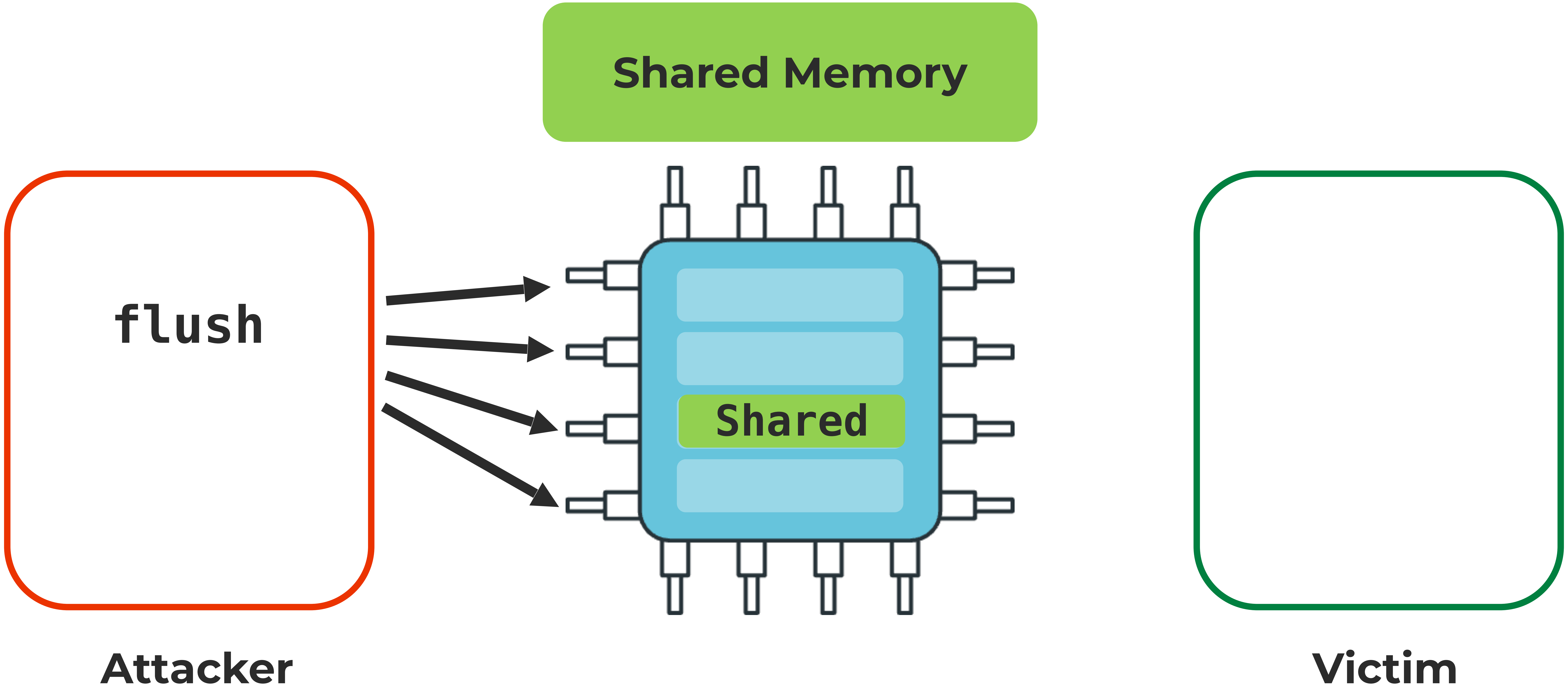

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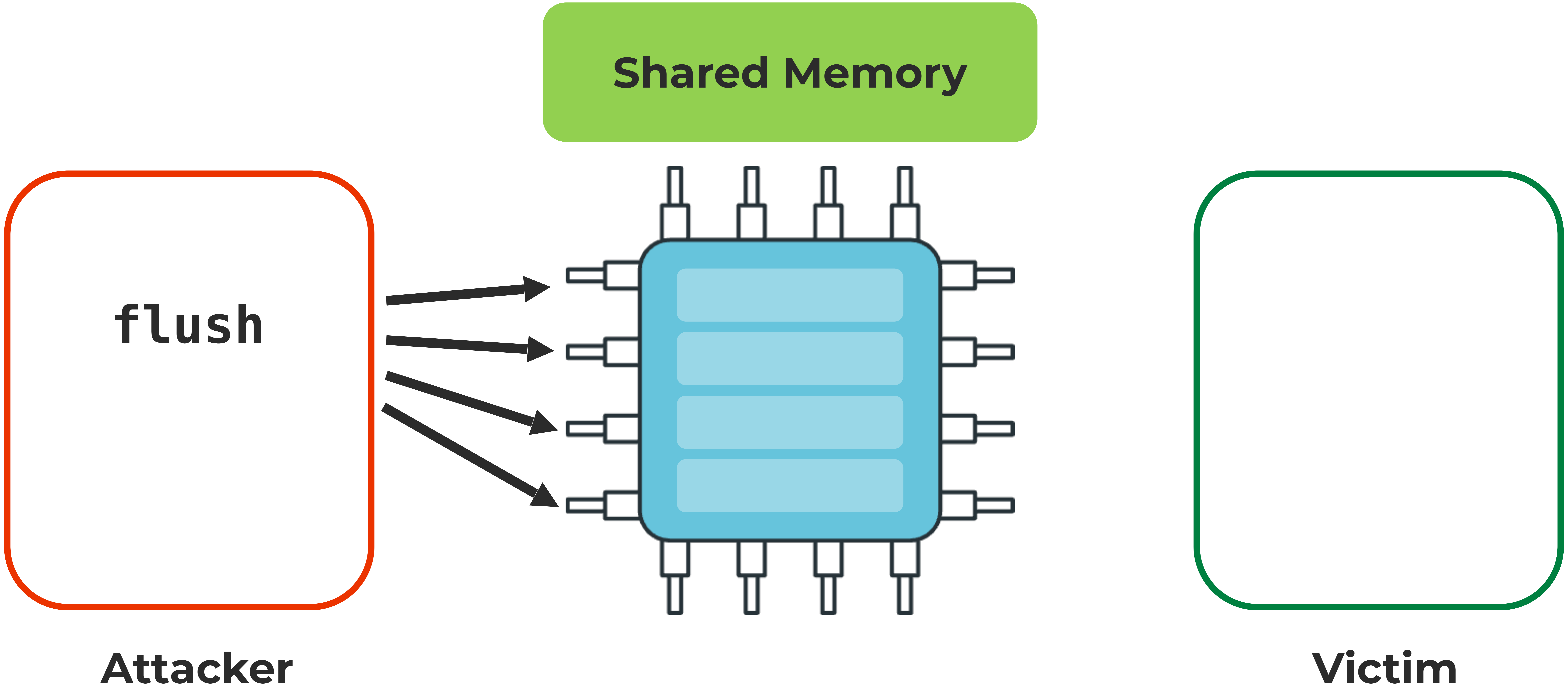

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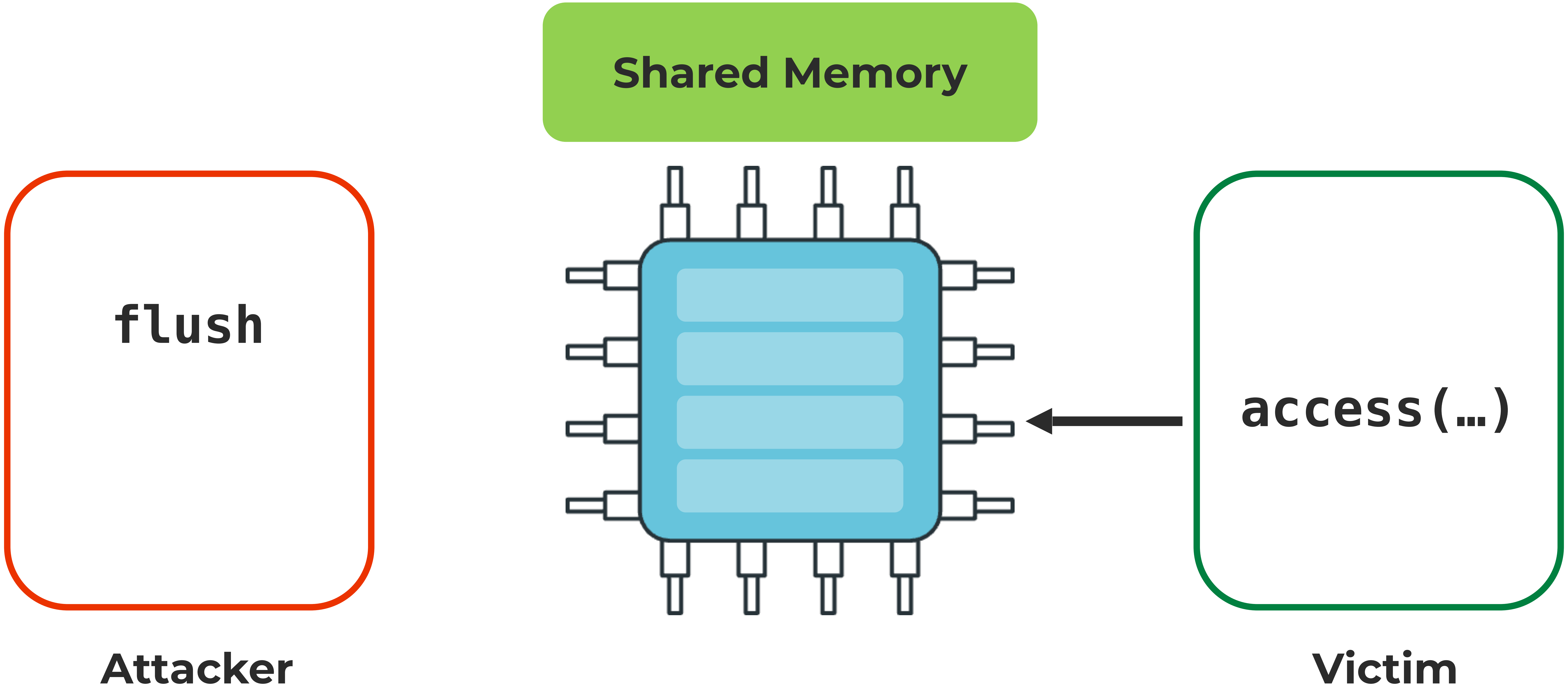

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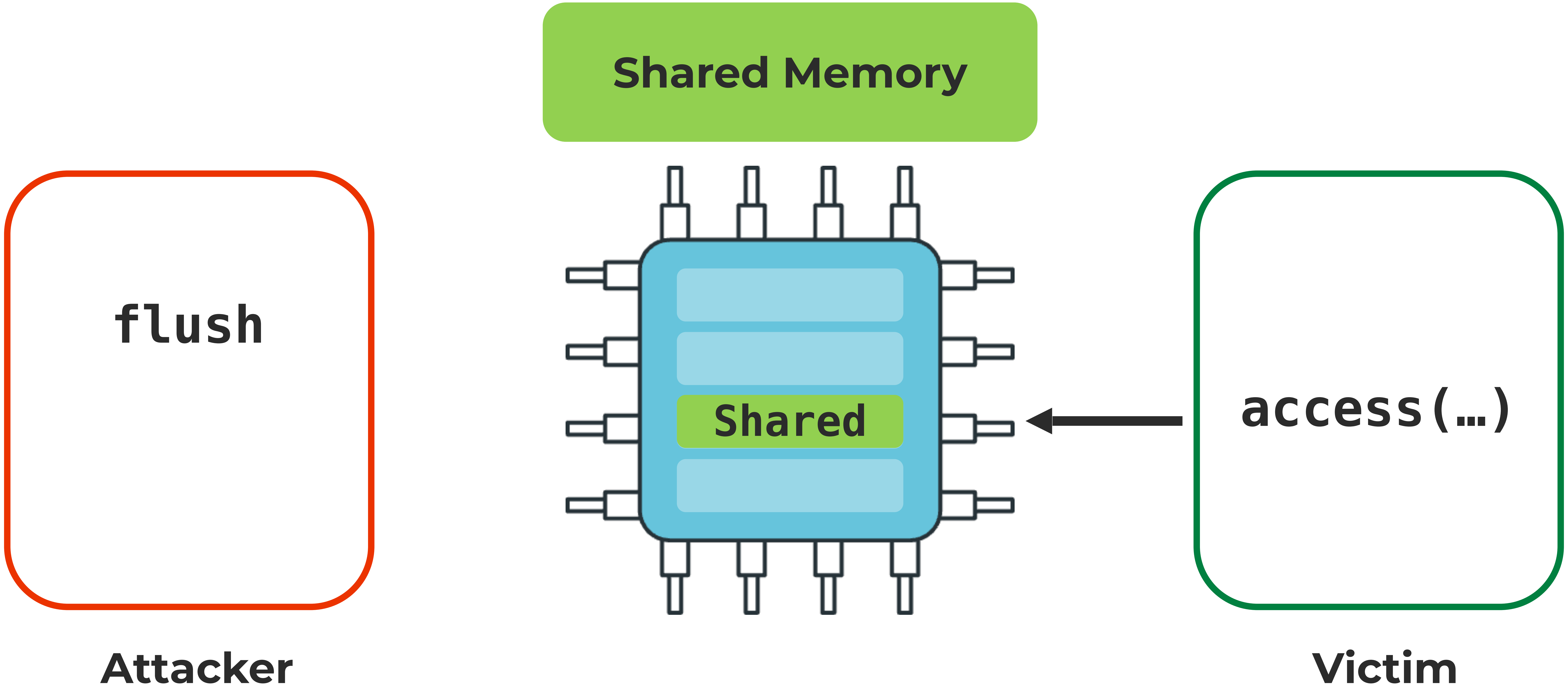
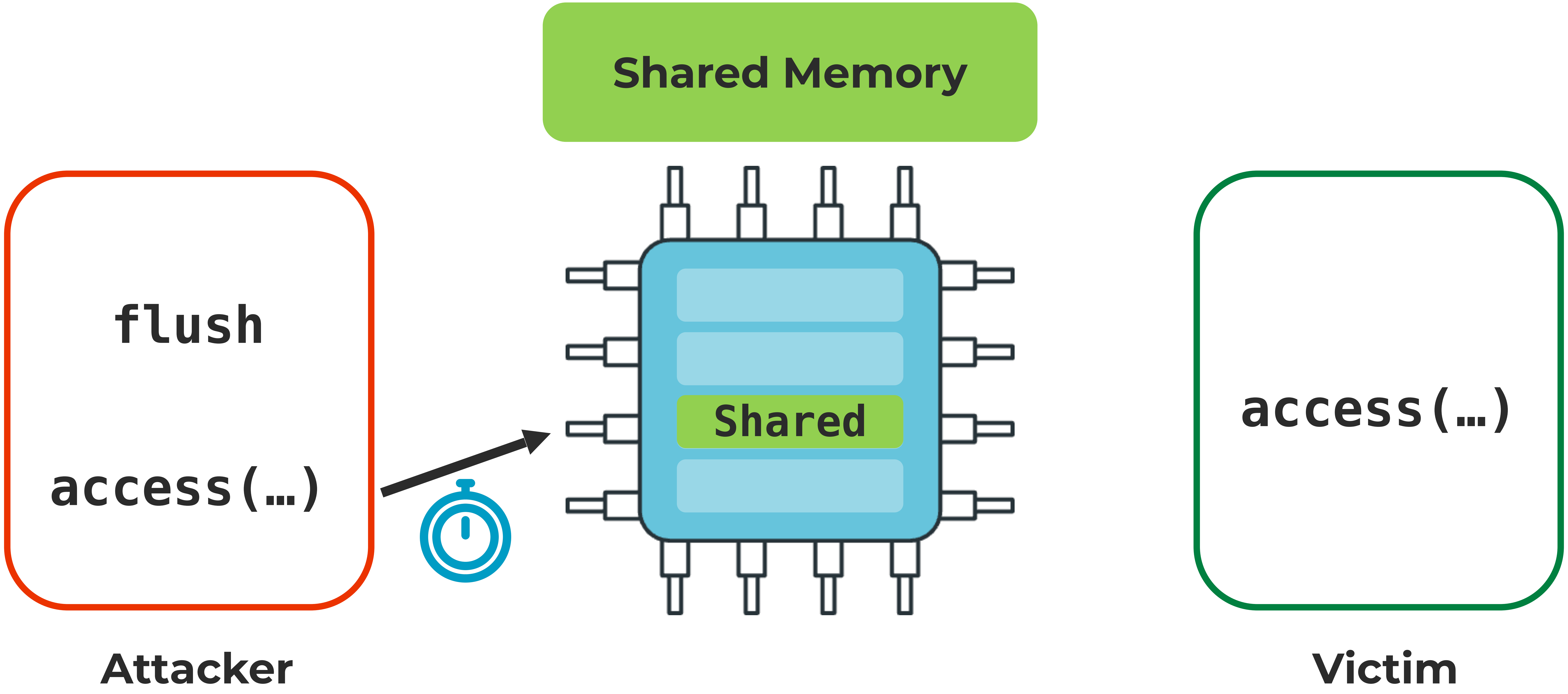


Flush+Reload



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→ **New Attack Variant:**

Flush+Fault

Flush+Fault

Attacker

```
if(secret){
    A();
} else {
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```

Victim

Flush+Fault

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I. Flush I-Cache with `fence.i`

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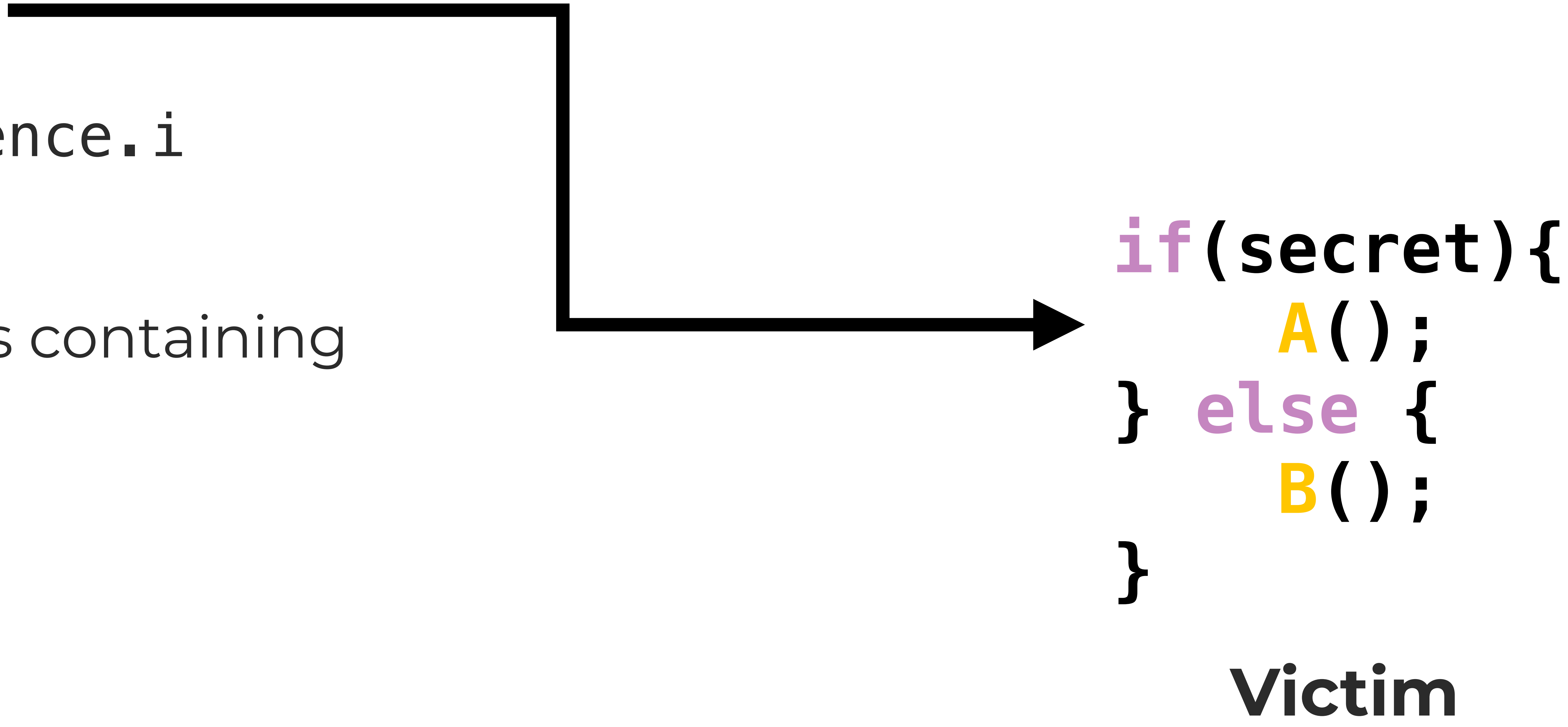

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II. Time jump to address containing victim cache line

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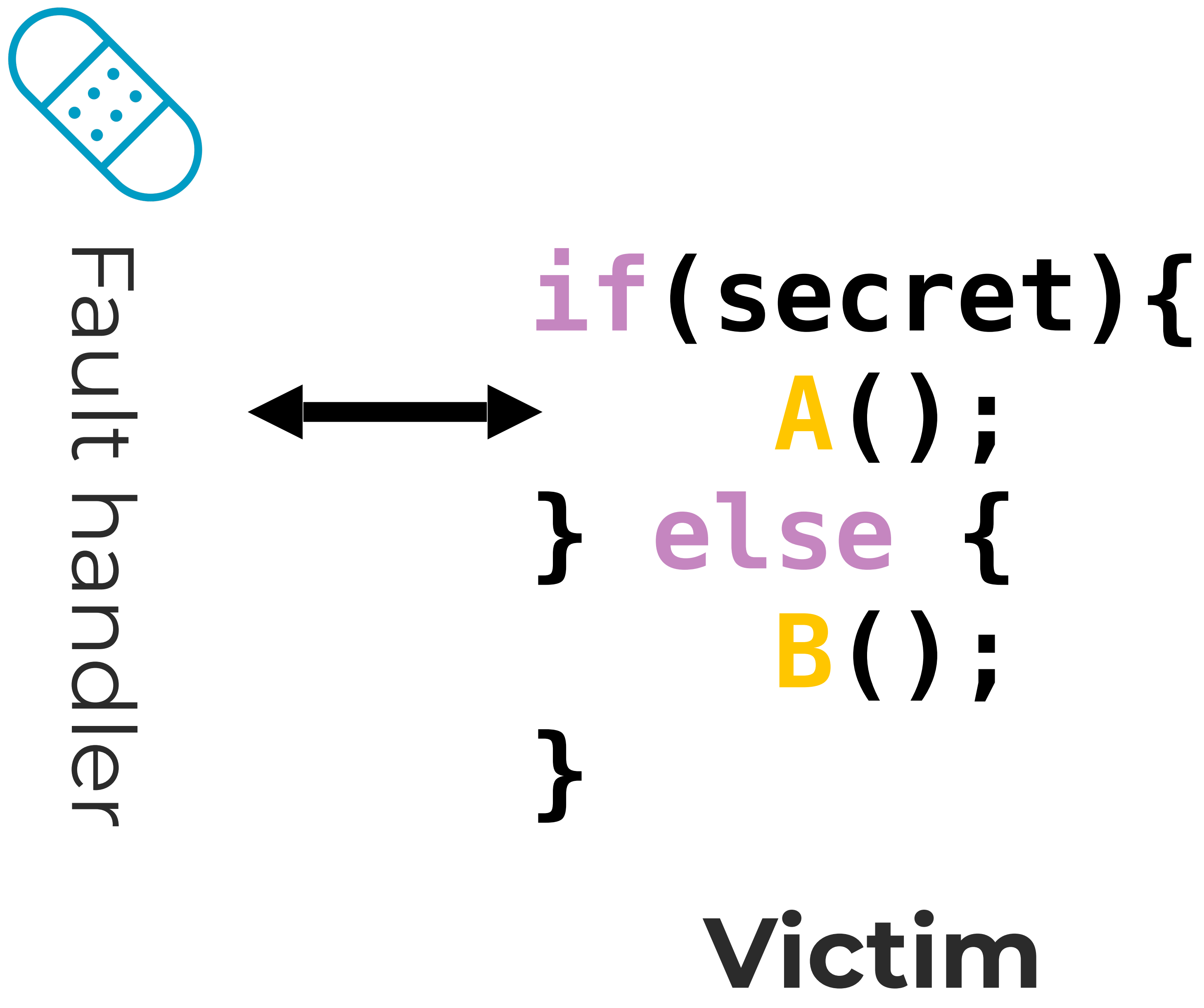

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Flush+Fault

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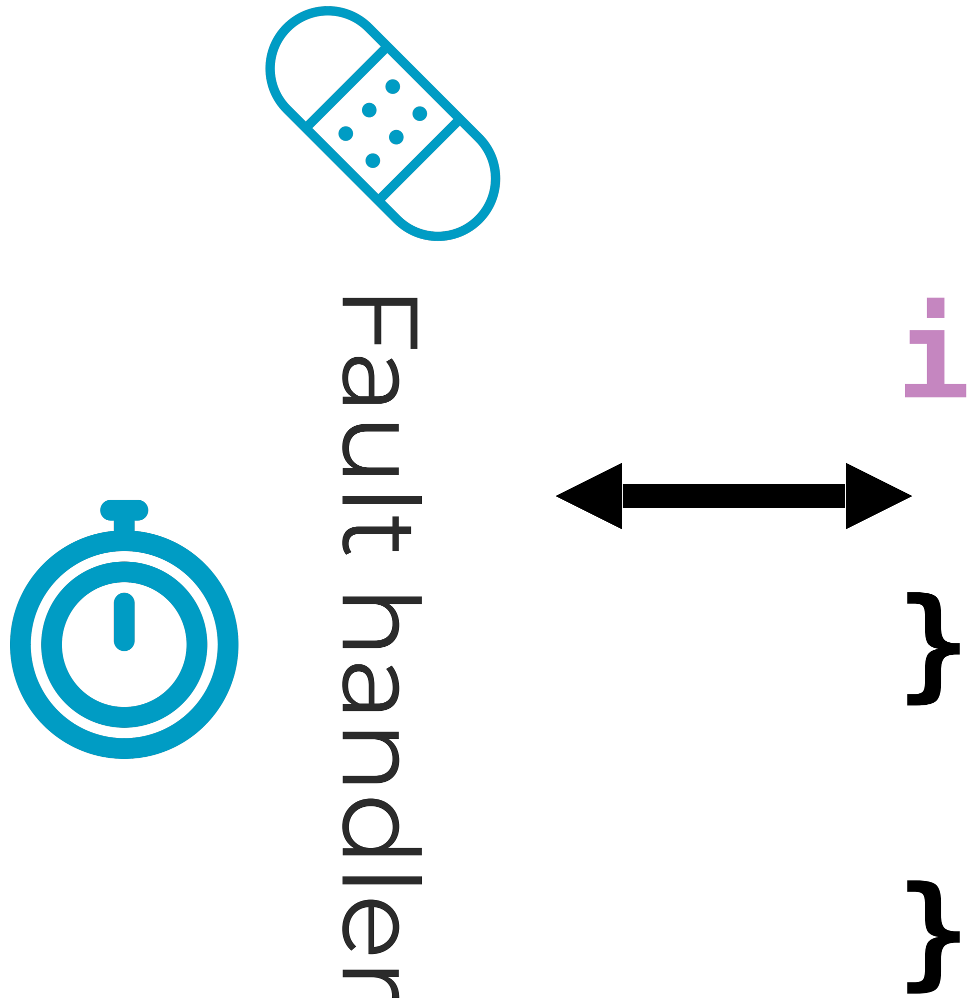
IV. Timing of fault handling leaks secret



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- **Adaptions are still possible**
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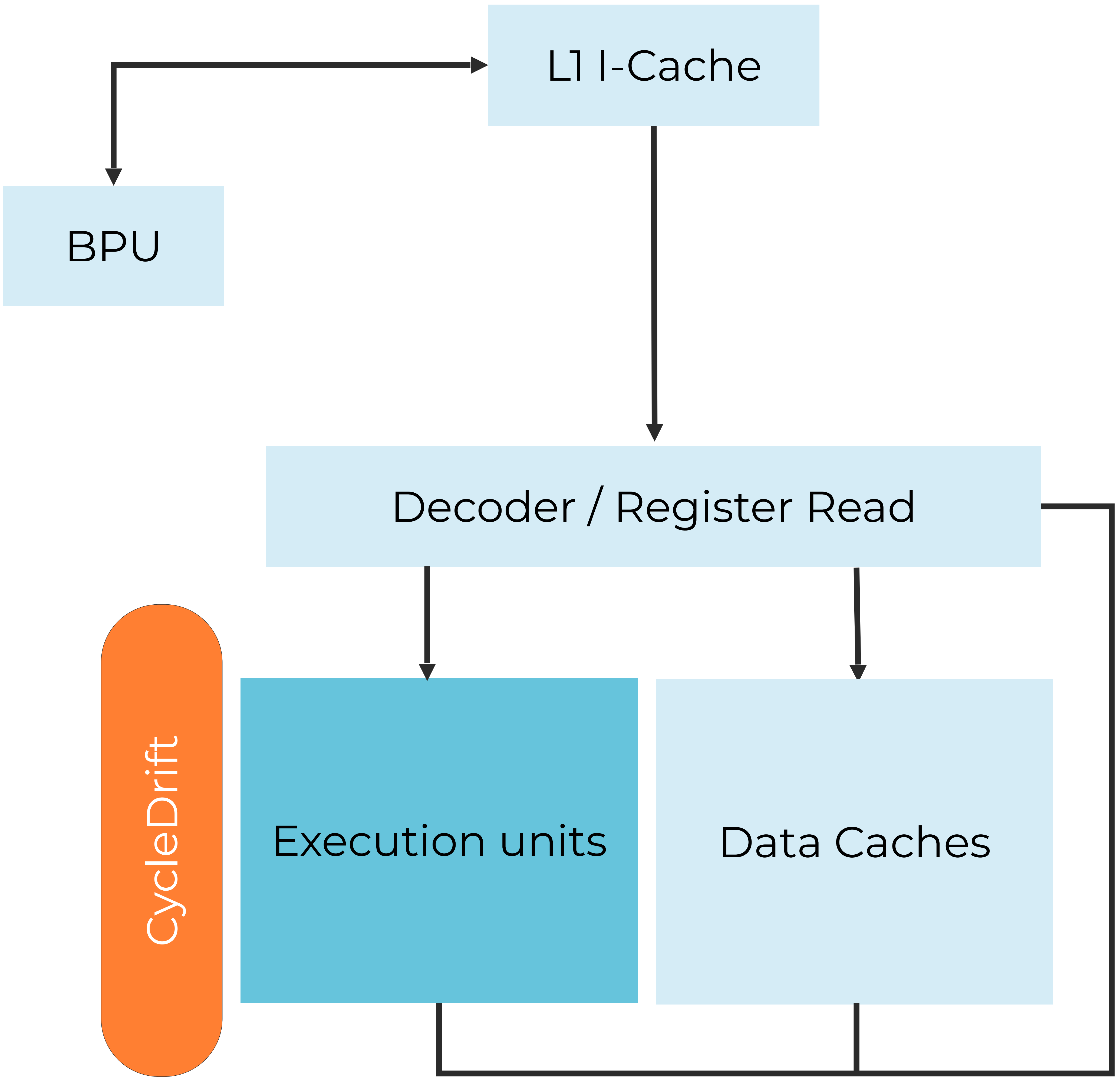
  - Data-cache Attacks

Nice! But What About the Other Attacks?

CPU Design: Performance Counters



What are Performance Counters?

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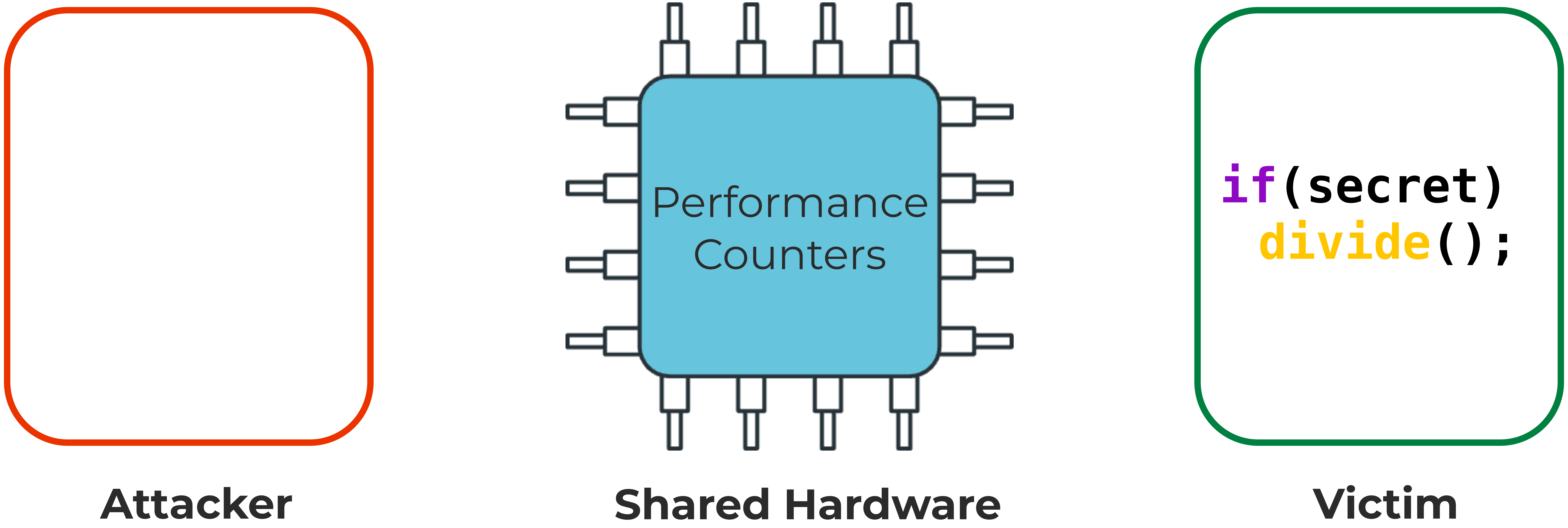

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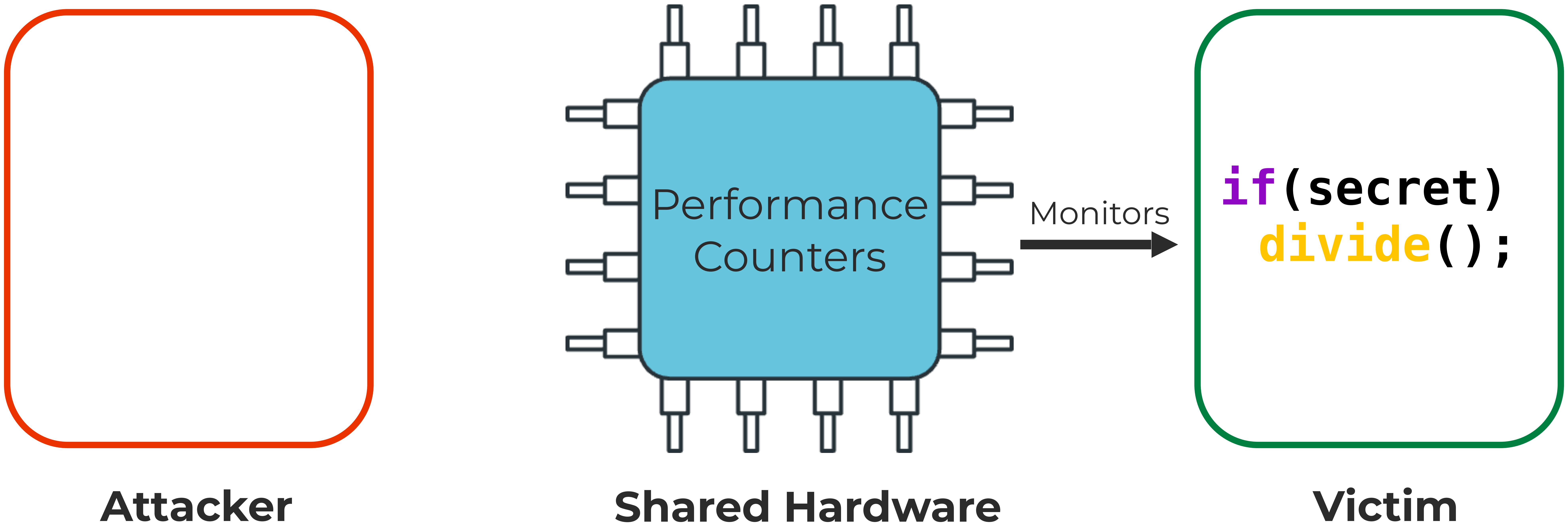

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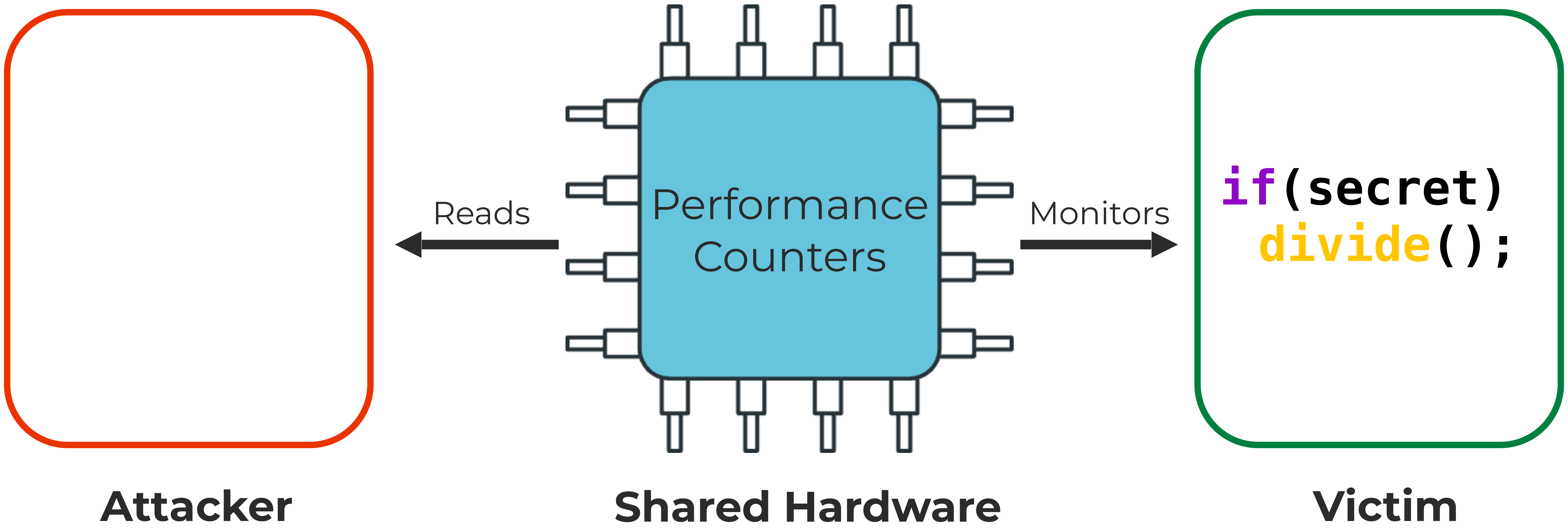

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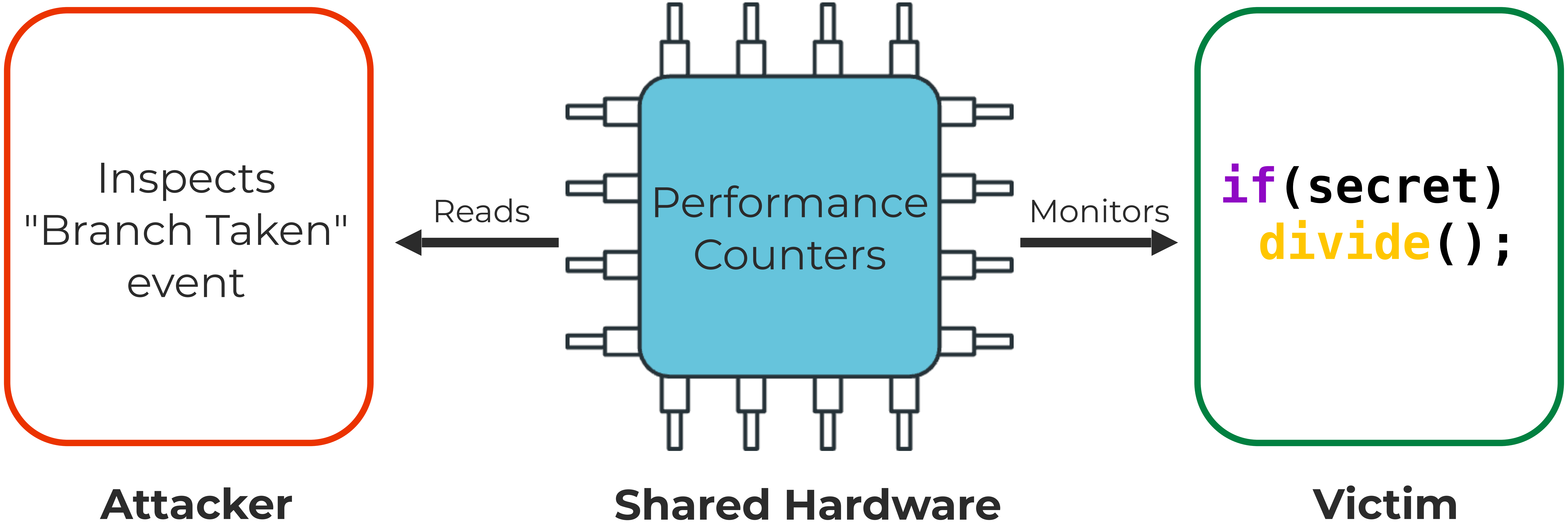

Inspects "Branch Taken" event

Reads

Performance Counters

Monitors

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Attacker

Shared Hardware

Victim

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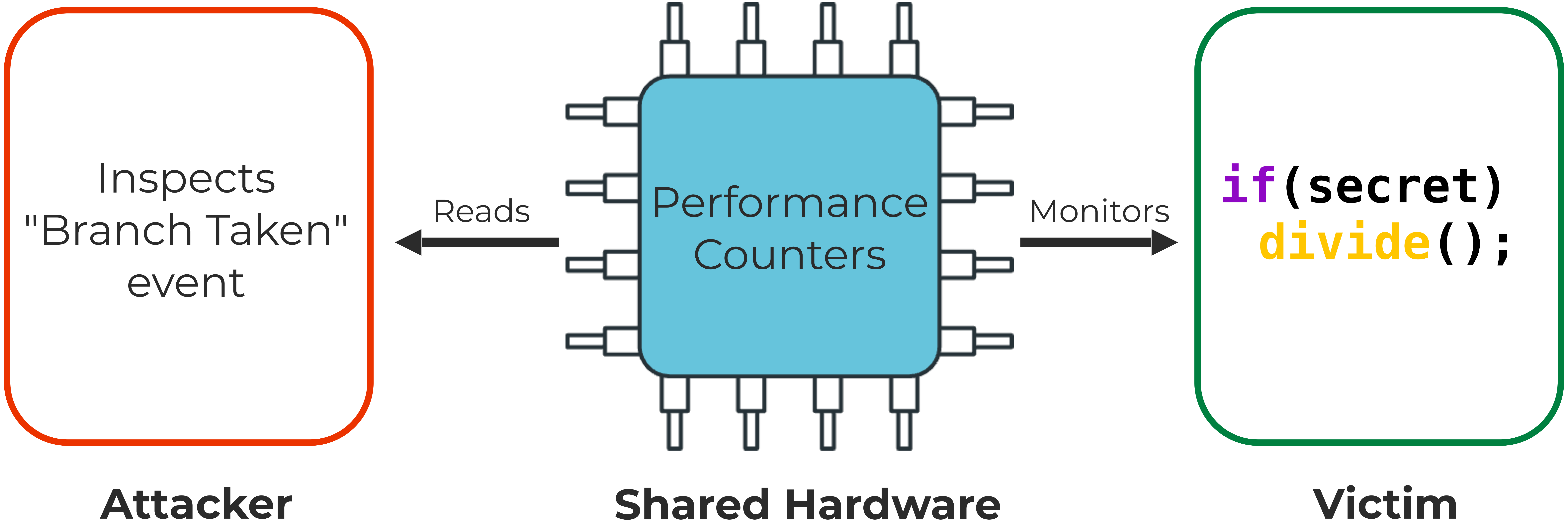

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Fix: Make the interface **privileged** (**root only**)!

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→ **Can we break that maybe?**

Live Demo: CycleDrift

demo@lab24: ~/demos
⌥⌘1

```
demo@lab24:~/demos$ ./kaslr-break
```

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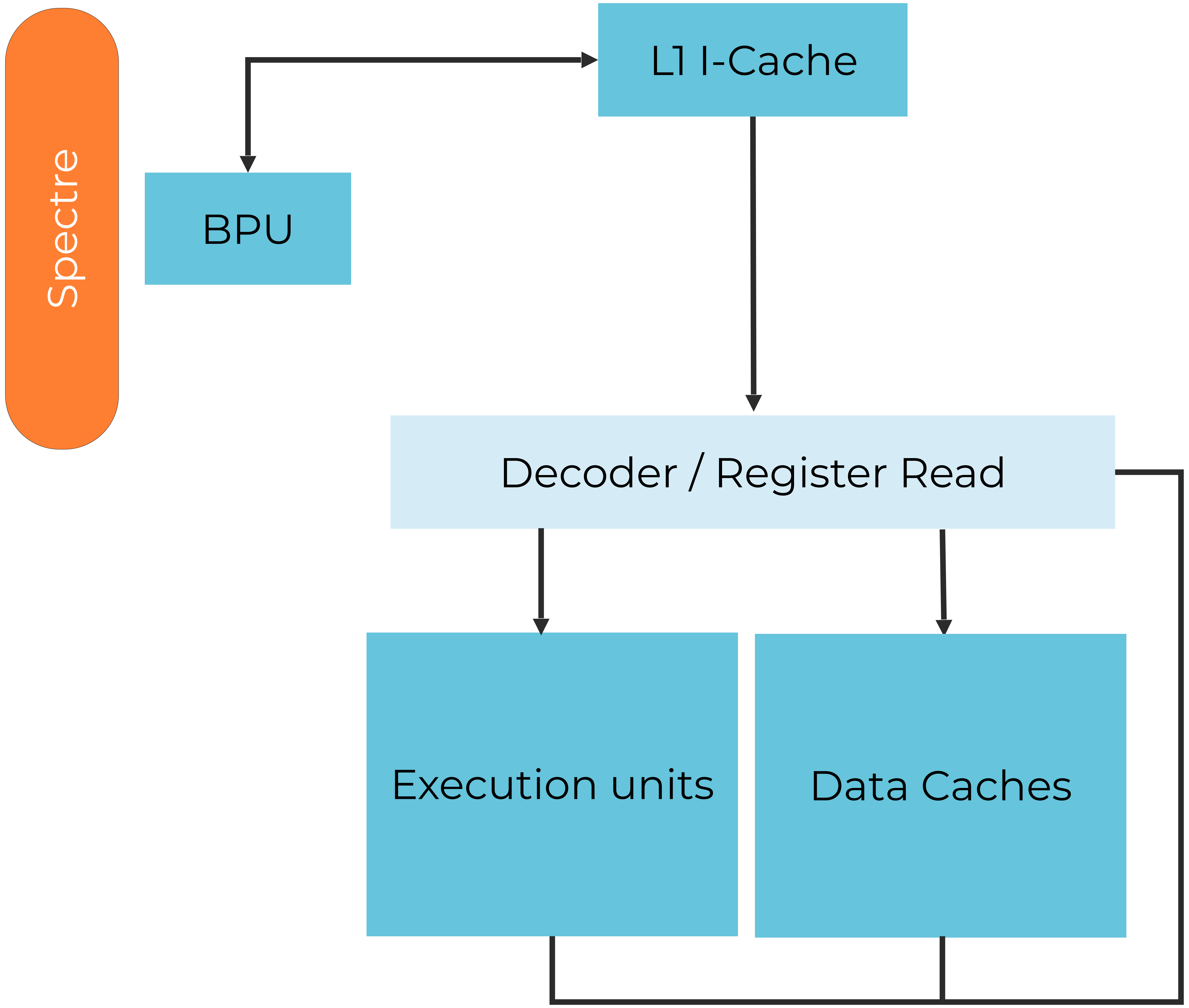
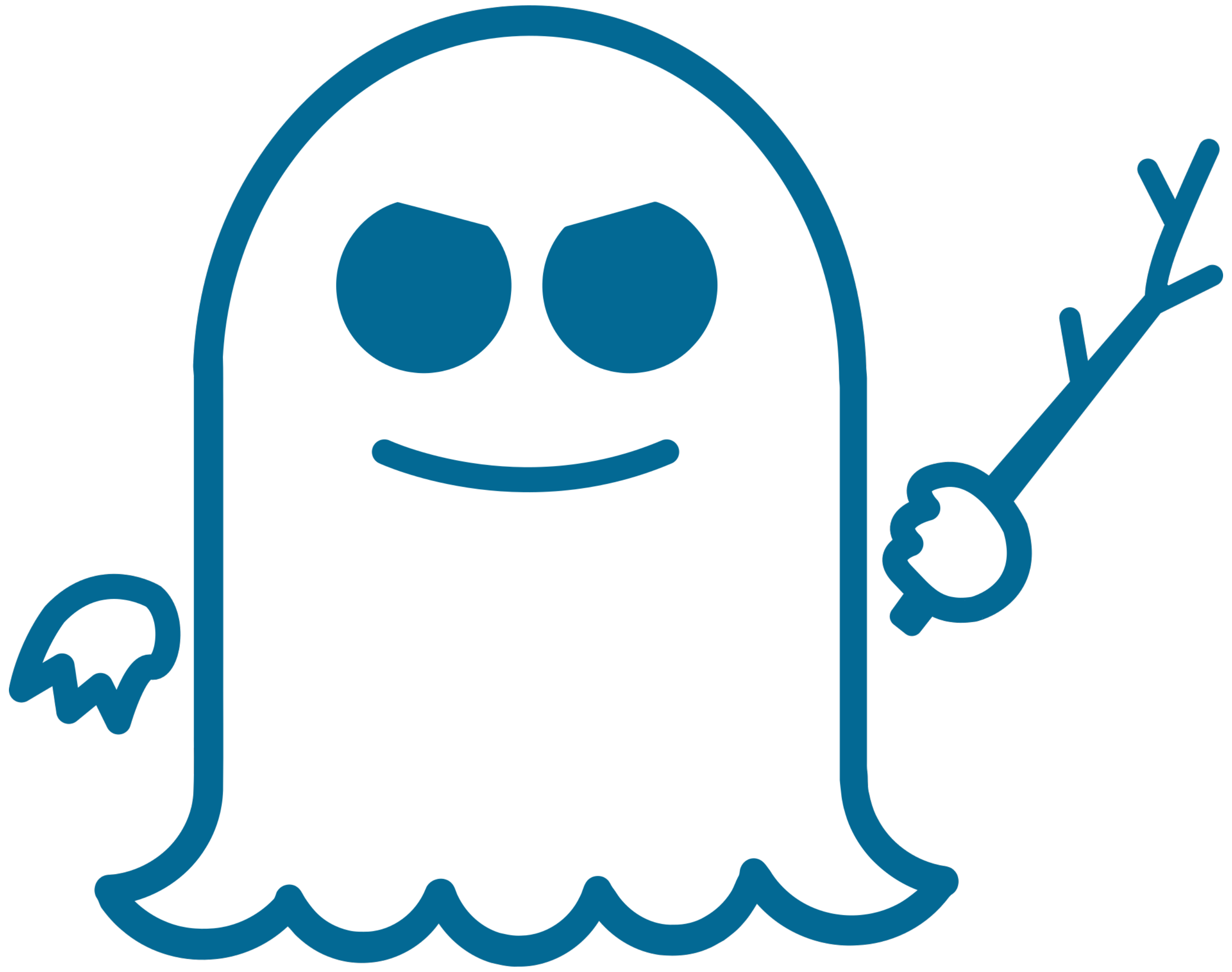
- More performance counters **will yield stronger attacks...**

CPU Design: Spectre





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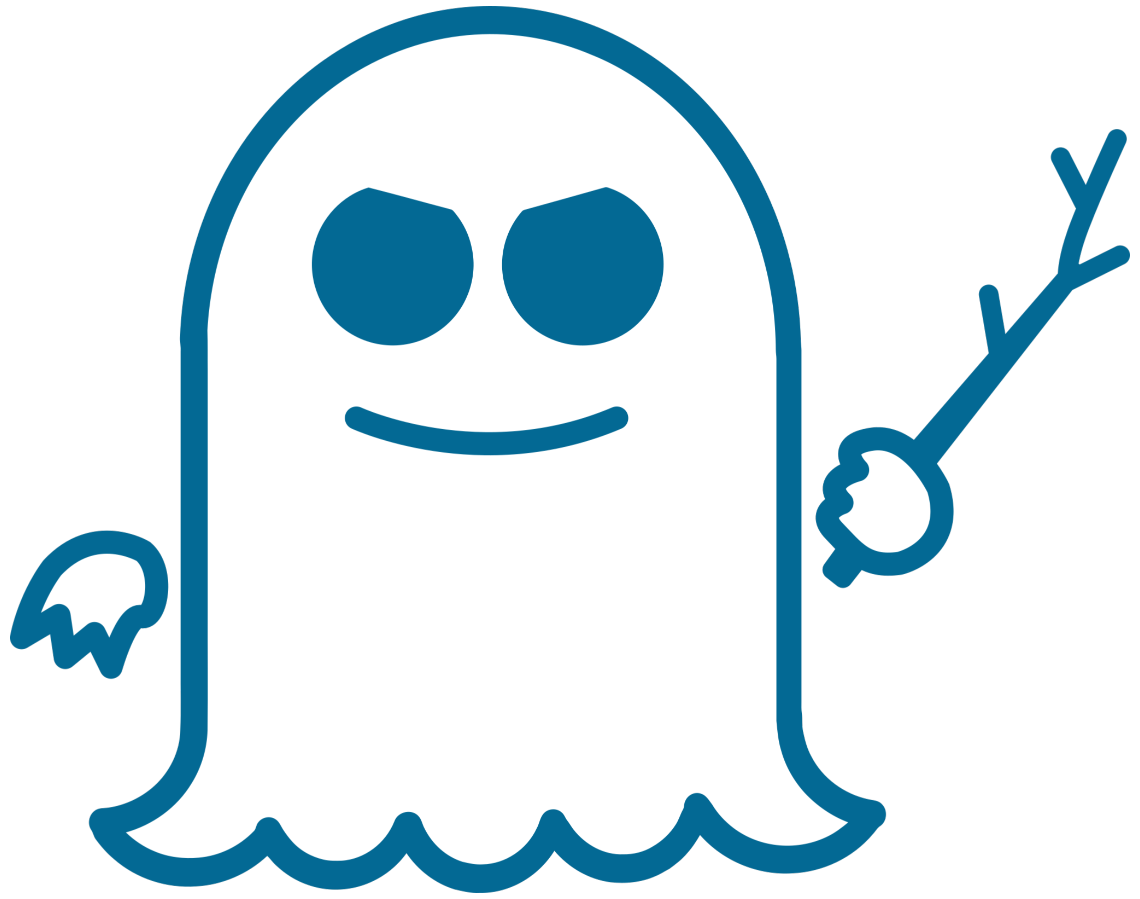
Spectre?



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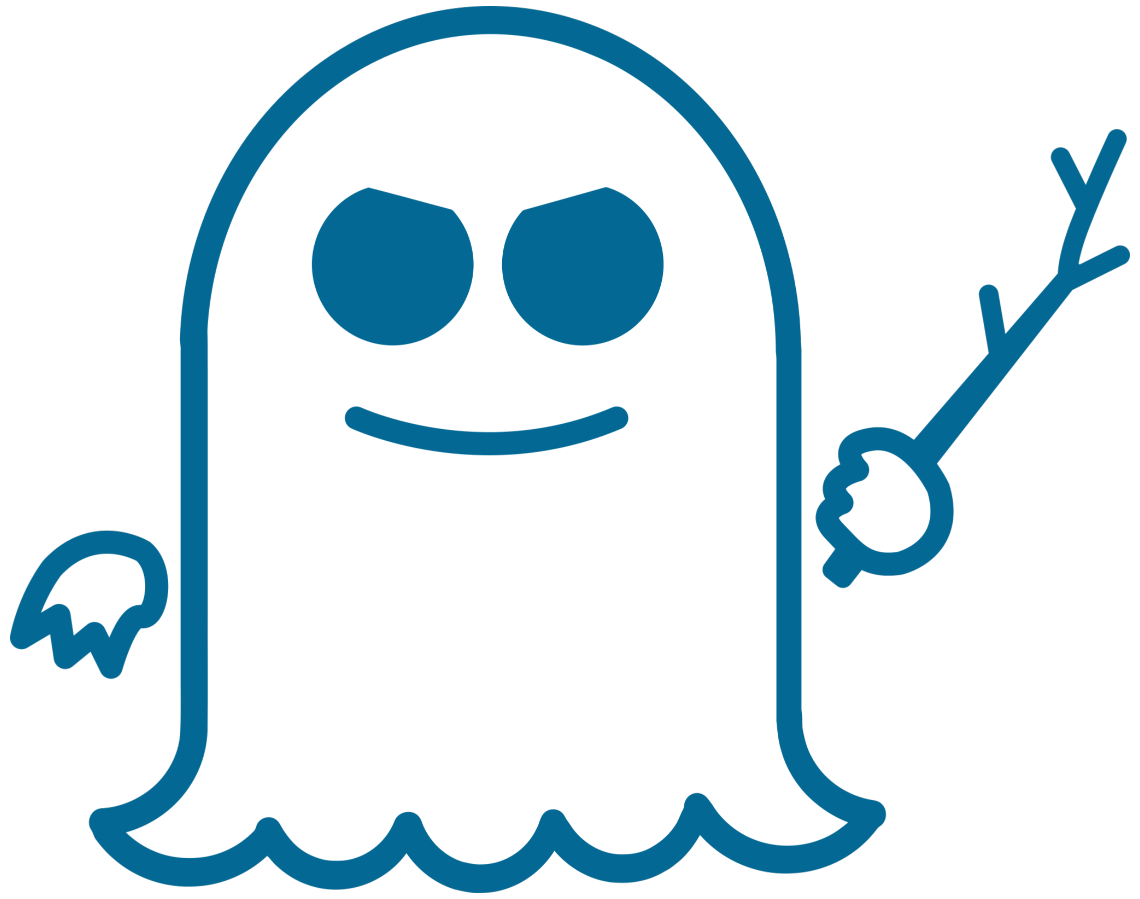
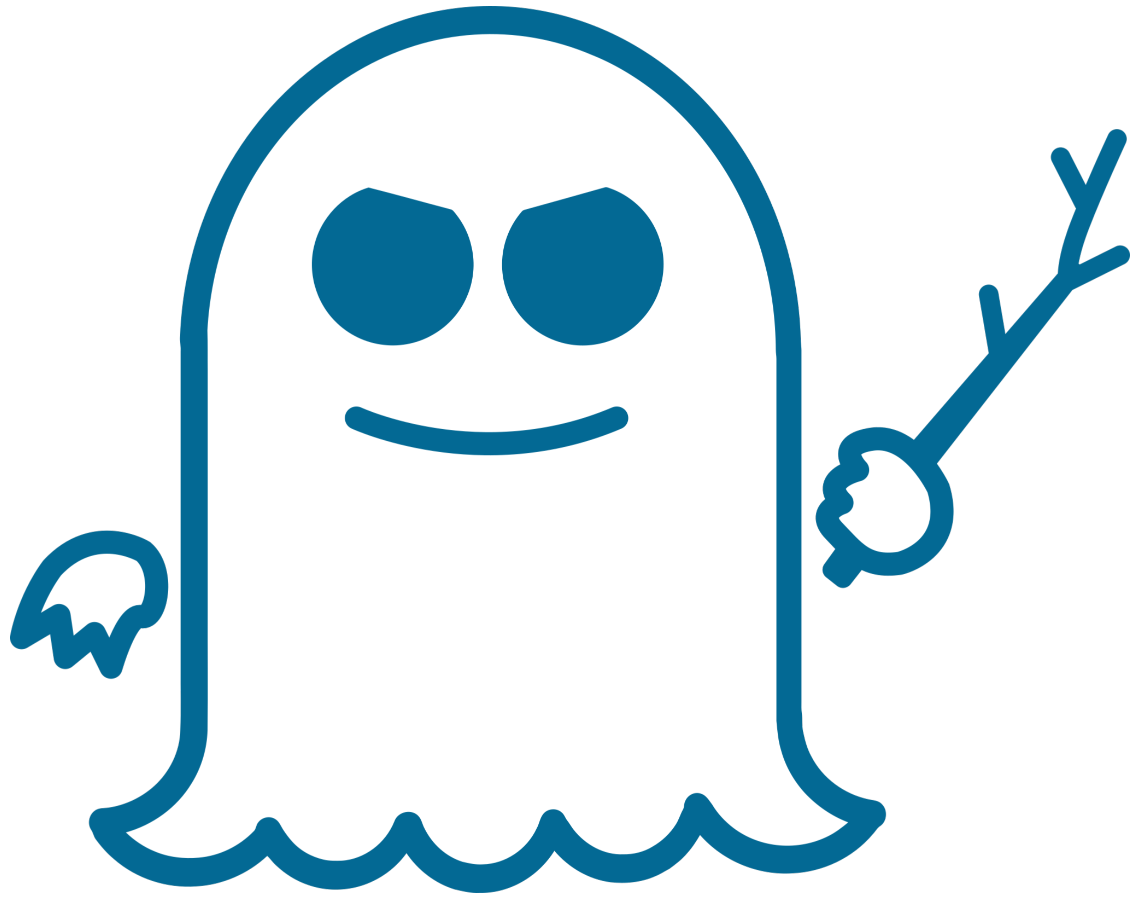
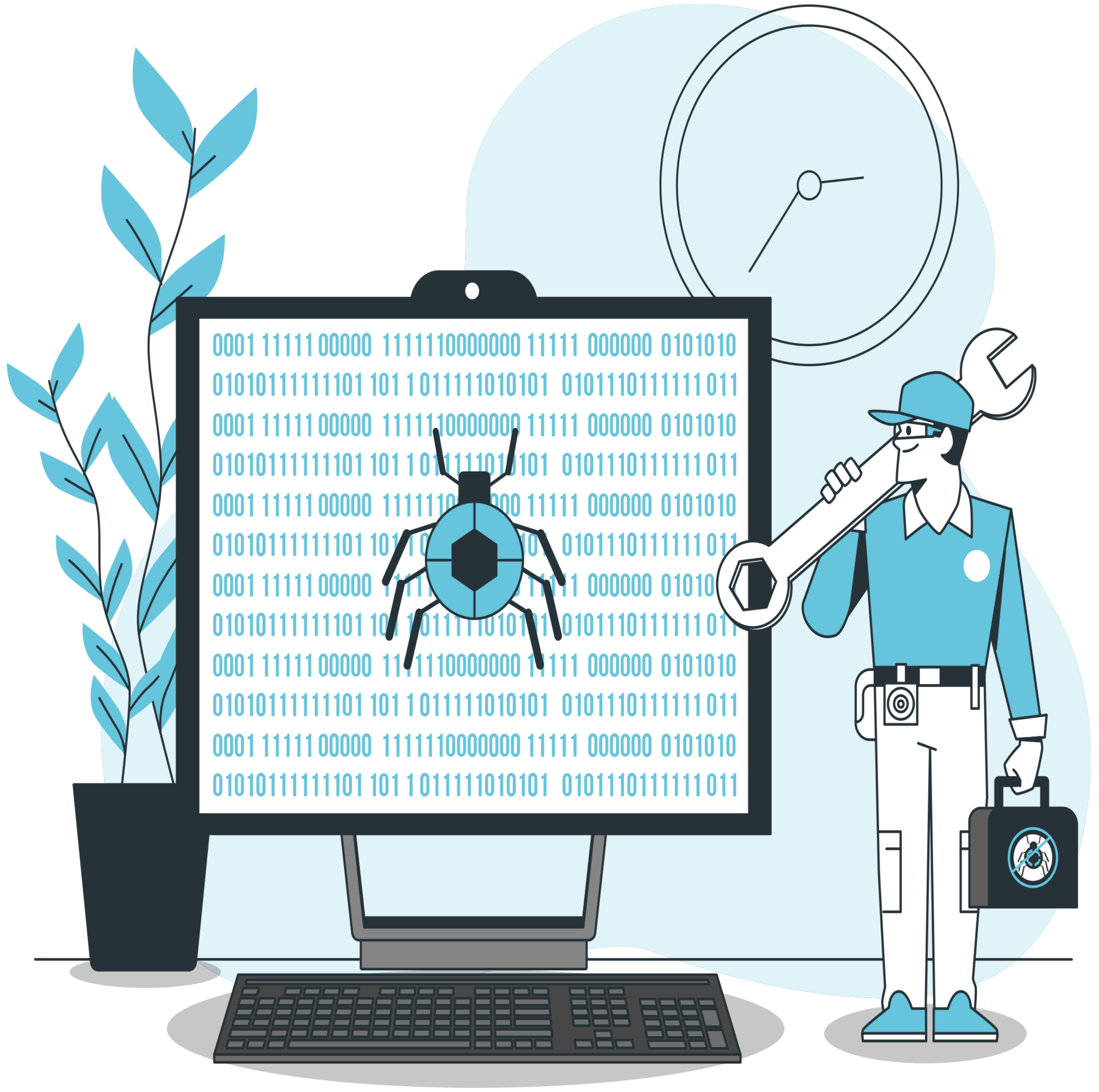


Spectre?

- Spectre **requires speculative execution**
- **Our RISC-V CPUs:** No support for speculative execution **(yet...)**





But there is speculative prefetching!

Cache+Time

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Victim

Cache+Time

- New **side channel** on the **instruction cache**

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fence.i

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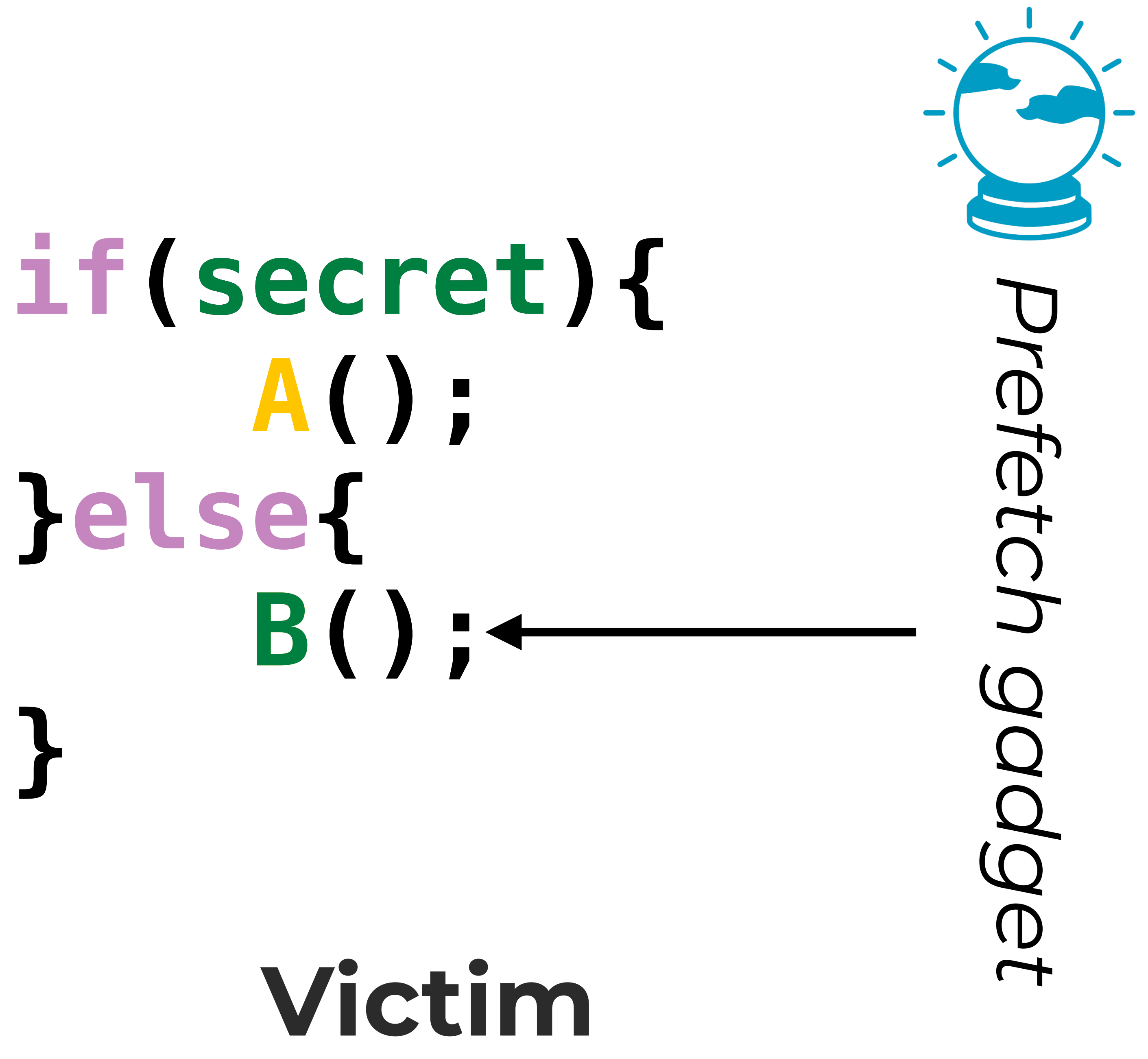

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Prefetch gadget

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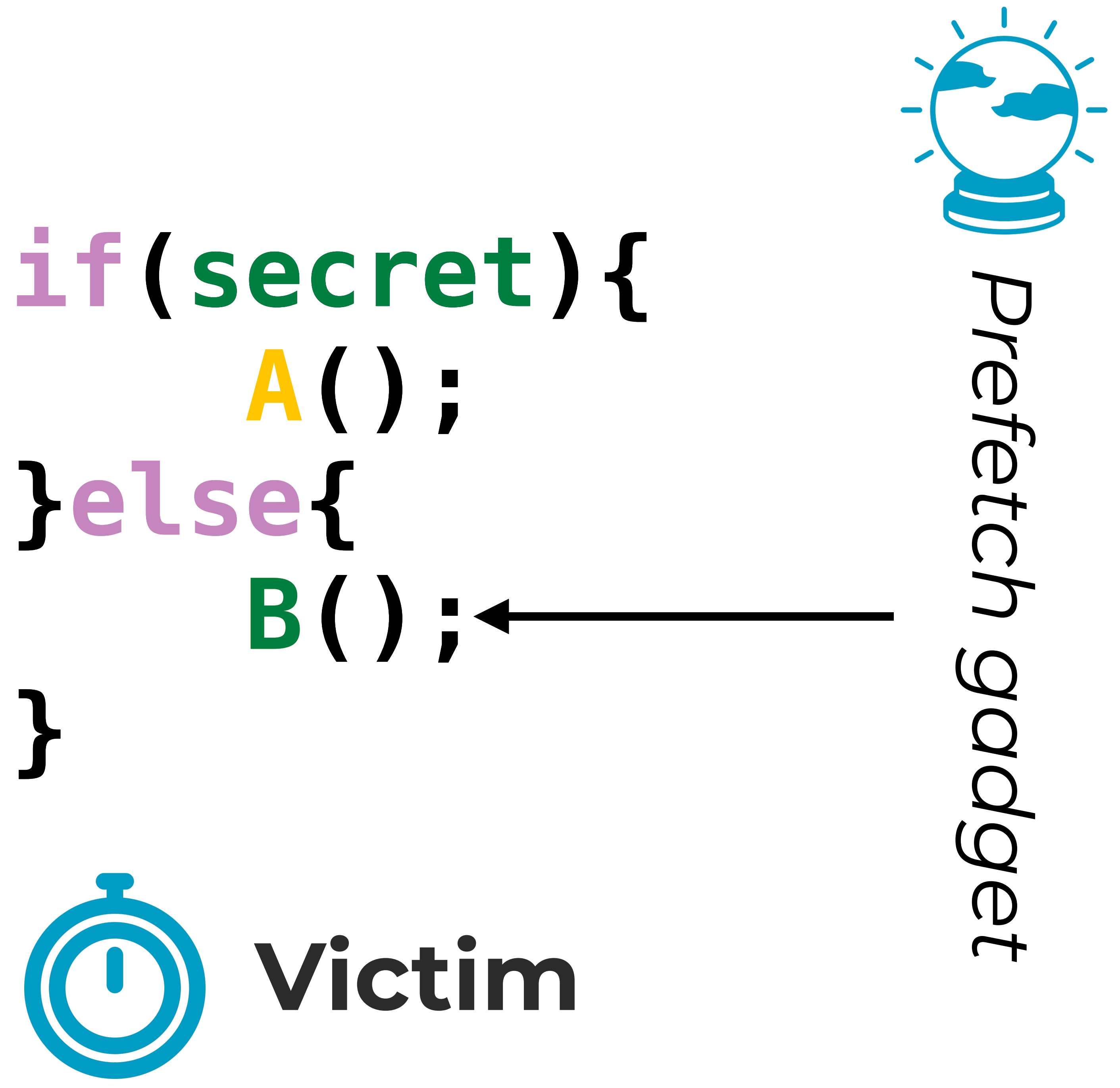

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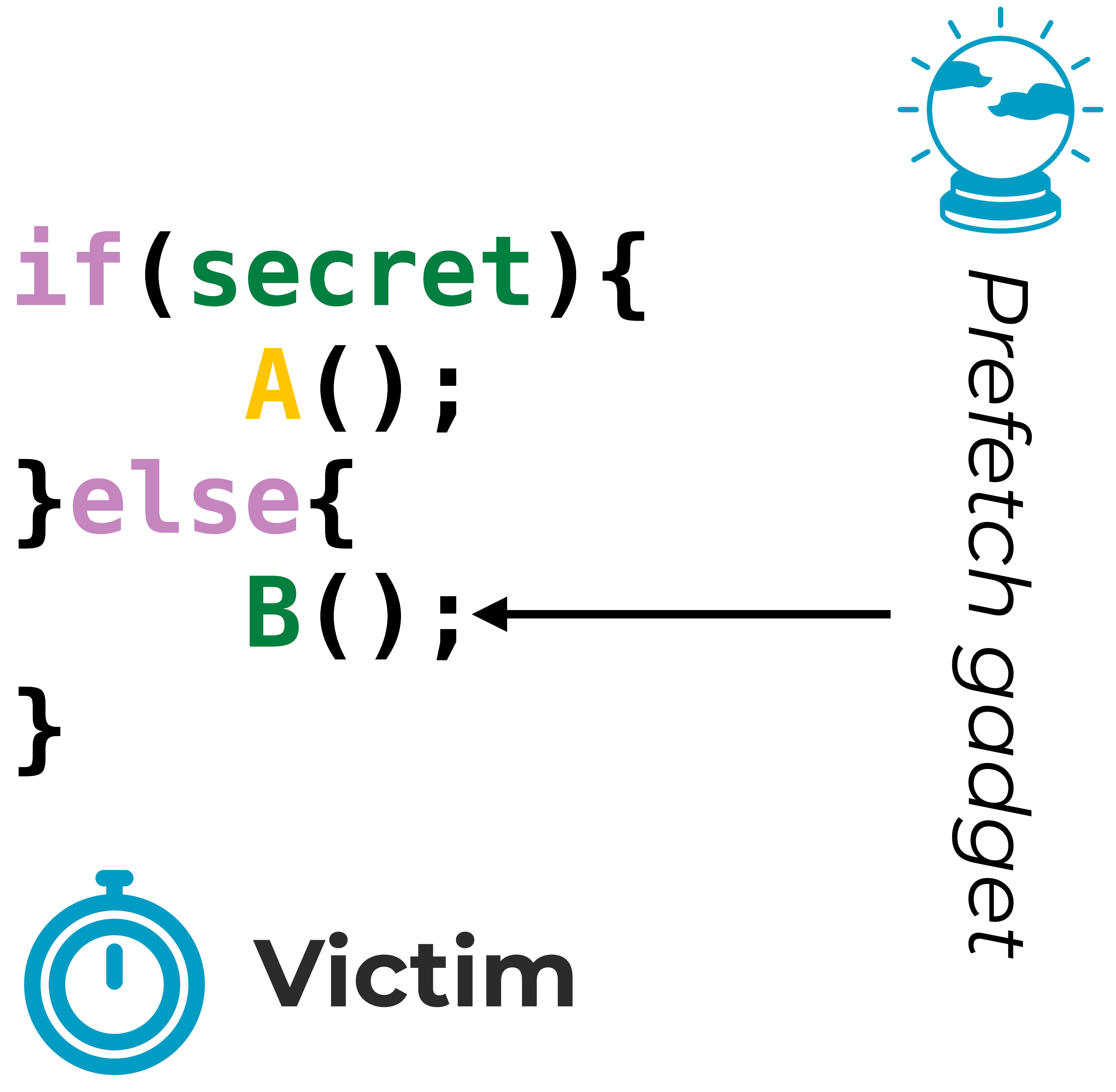
➡ **Speculative prefetching is exploitable**



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Surpise Demo: Spectre is fixed? Right?

beagle@lab46: ~/specre-riscv

⌥⌘1

```
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```

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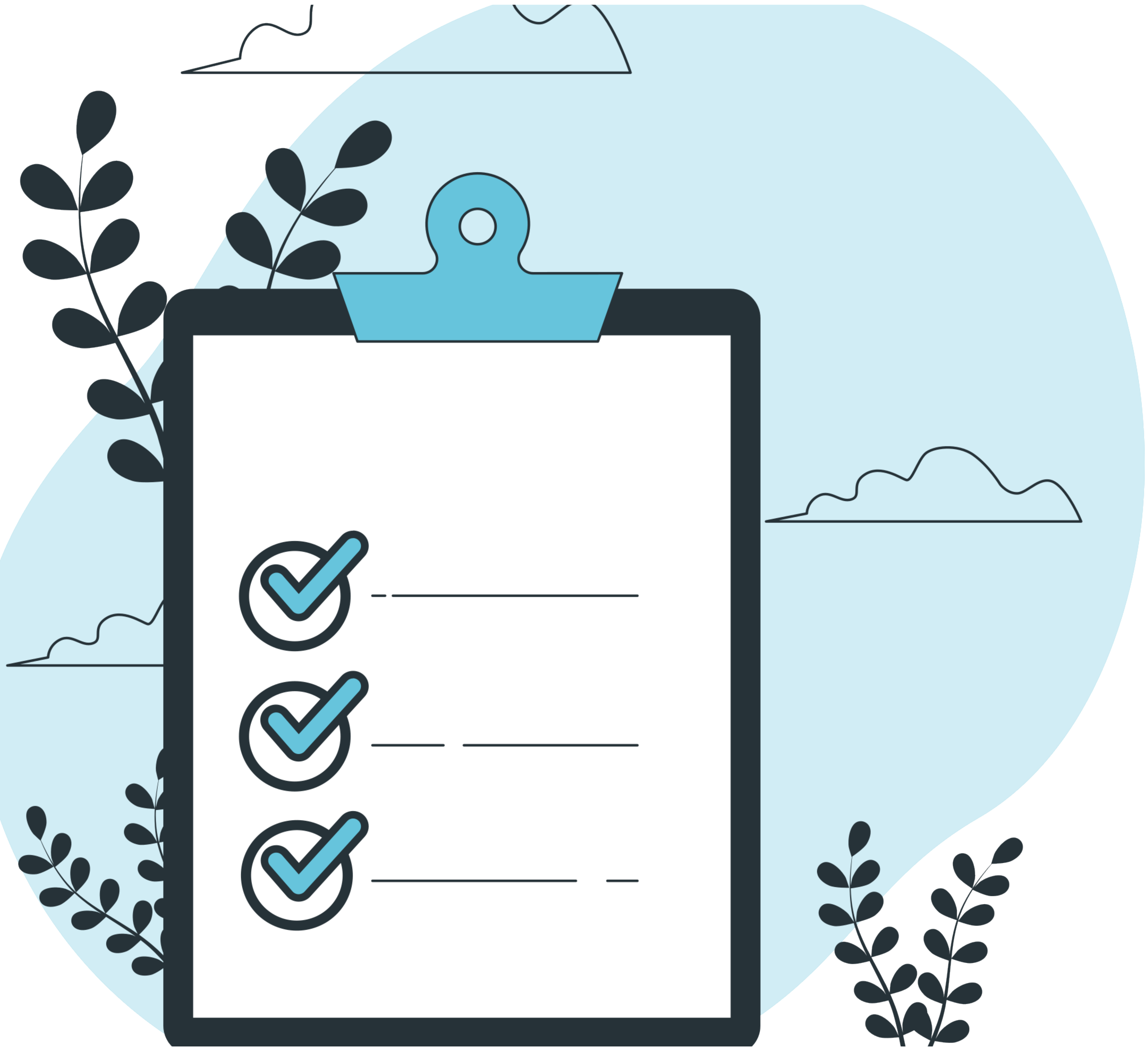
➡ **More optimized cores (C910) are more vulnerable**



Conclusion

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Want to Play Around with the Code?

https://github.com/cispa/Security-RISC

Takeaways

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More (optimized) RISC-V cores on the way

@____salmon____ @weber_daniel

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↓

Security Research on RISC-V hardware **is essential!**

@____salmon____ @weber_daniel

CISPA
HELMHOLTZ CENTER FOR
INFORMATION SECURITY

A Security RISC?

The State of Microarchitectural Attacks on RISC-V

Lukas Gerlach, **Daniel Weber**, Michael Schwarz | BlackHat EU 2023