



Collide+Power

The Evolution of Software-based Power Side-Channels Attacks

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6th December 2023



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 - Software-based power side channels
 - Software-based fault attacks
 - Trusted execution environments



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Software-based Power Side Channels



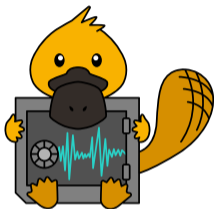
Software-based Power Side Channels

- **Specific** targets: Algorithms



Software-based Power Side Channels

- **Specific** targets: Algorithms
- Leak edge cases



Software-based Power Side Channels

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Transient Execution Attacks



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- **Generic** targets: CPU components



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Transient Execution Attacks

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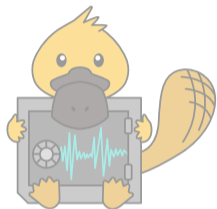


Software-based Power Side Channels

- **Specific** targets: Algorithms
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Transient Execution Attacks

- **Generic** targets: CPU components
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Software-based Power Side Channel Attacks

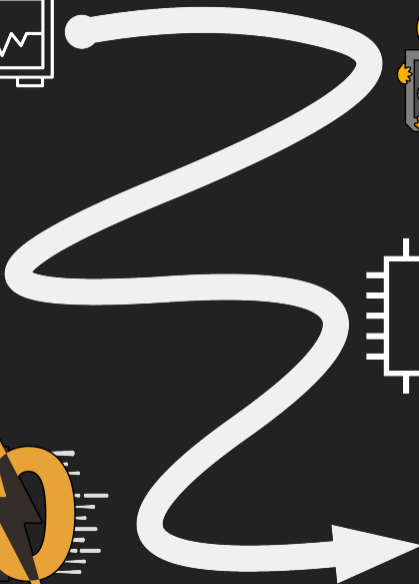
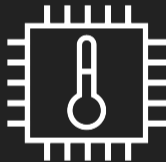
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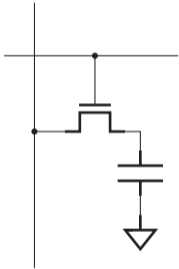
Execution Attacks

- **Generic** targets: CPU components
- Leak arbitrary data
- **Agnostic** to side channels

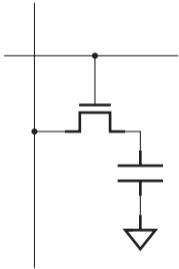


Can we build a **generic** software-based
power side-channel attack **independent** of
the targeted application?

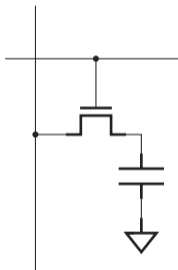




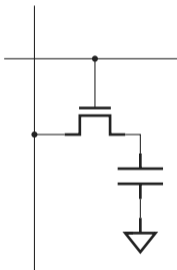
- Complementary **M**etal **O**xide **S**emiconductor



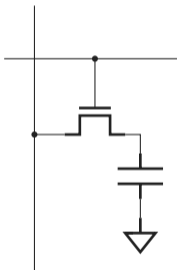
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- **L**ow power consumption



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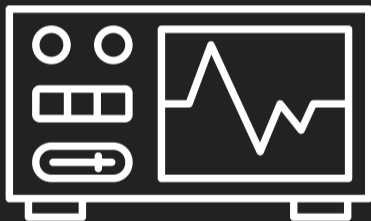


- Complementary **Metal Oxide Semiconductor**
- **Low** power consumption
- Depends on:
 - **Instruction** that is executed

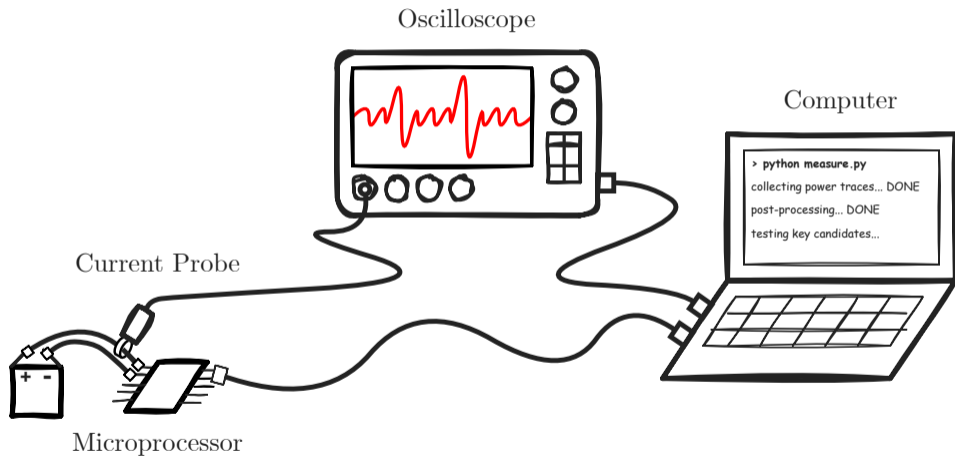


- Complementary **Metal Oxide Semiconductor**
- **Low** power consumption
- Depends on:
 - **Instruction** that is executed
 - **Data** that is being processed

Traditional Power Side Channels



Power Side Channel - Setup



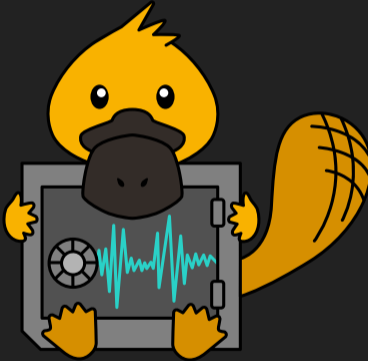


How can we **measure** the power consumption of a modern CPU?

How would we ever do this **remotely**?

```
→ ~      cat /sys/class/powercap/intel-rapl:0/intel-rapl:0:0/energy_uj  
90211251602
```

PLATYPUS¹



¹Moritz Lipp, Andreas Kogler, David Oswald, Michael Schwarz, Catherine Easdon, Claudio Canella, and Daniel Gruss. PLATYPUS: Software-based Power Side-Channel Attacks on x86. In: S&P. 2021.



Unprivileged power meter



Unprivileged power meter



No physical access

Running Average Power Limit (RAPL)



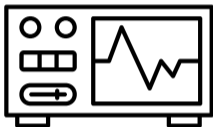
Unprivileged power meter

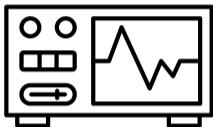


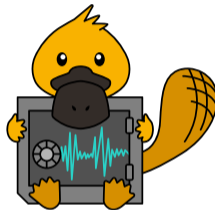
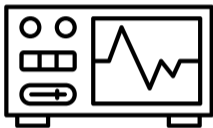
No physical access



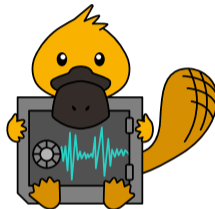
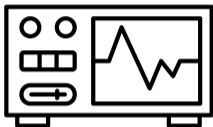
Low refresh rate



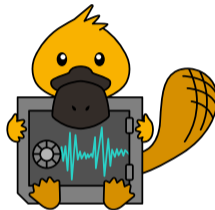
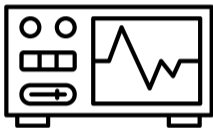




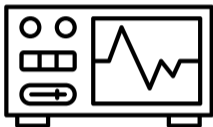
- **Full Control**



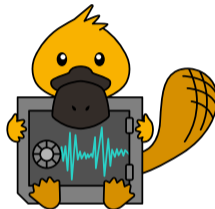
- **Full** Control
- **High** timing resolution



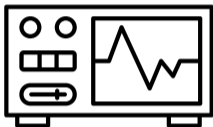
- **Full** Control
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- **Multiple** samples per instruction



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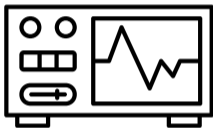
- **No** control, just a register



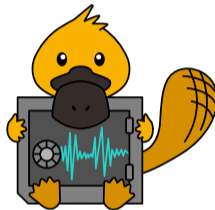
- **Full** Control
 - **High** timing resolution
- **Multiple** samples per instruction



- **No** control, just a register
- **Low** timing resolution

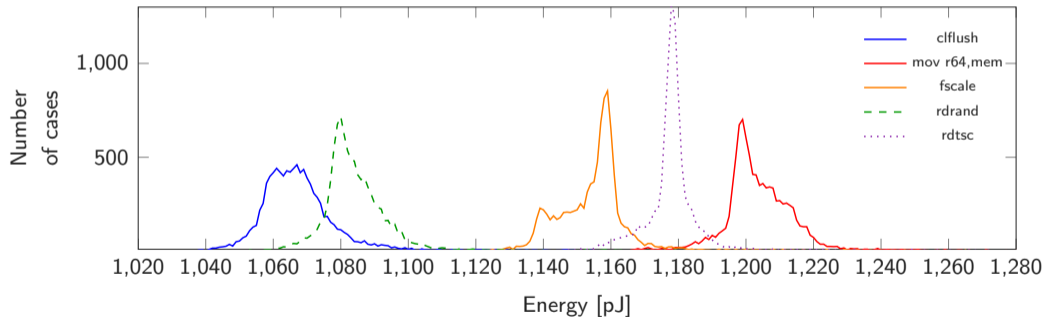


- **Full** Control
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- **Multiple** samples per instruction

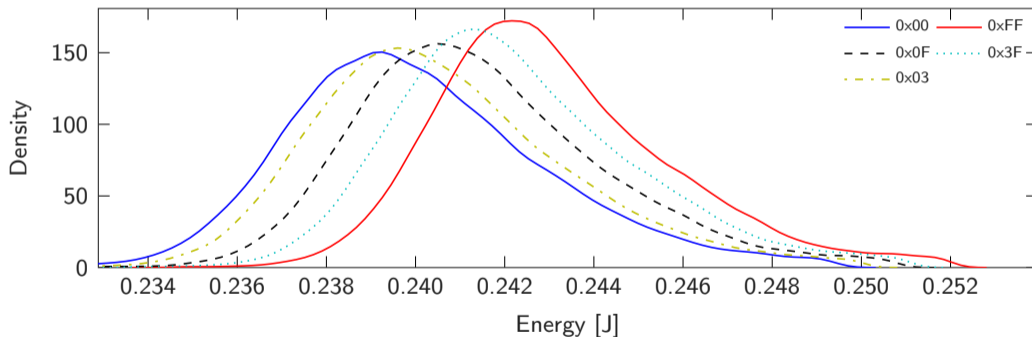


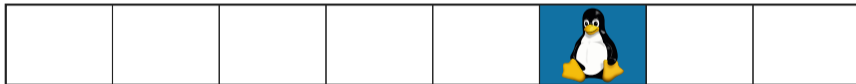
- **No** control, just a register
 - **Low** timing resolution
- **Single** sample per multiple instructions

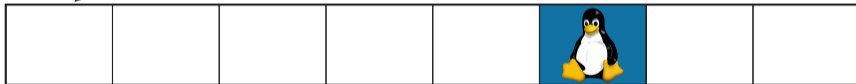
- Measure the **energy consumption** of **different instructions**

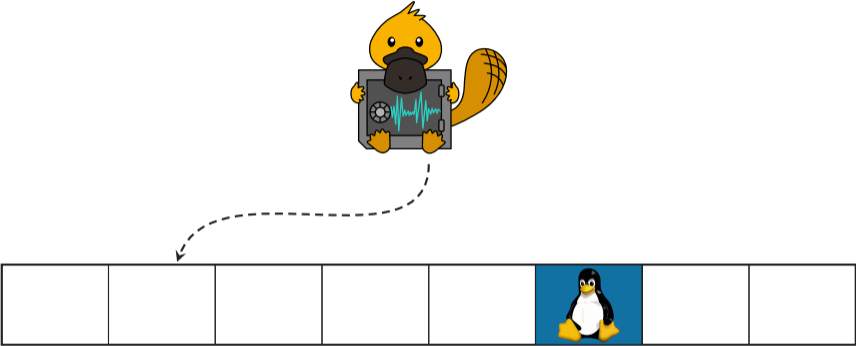


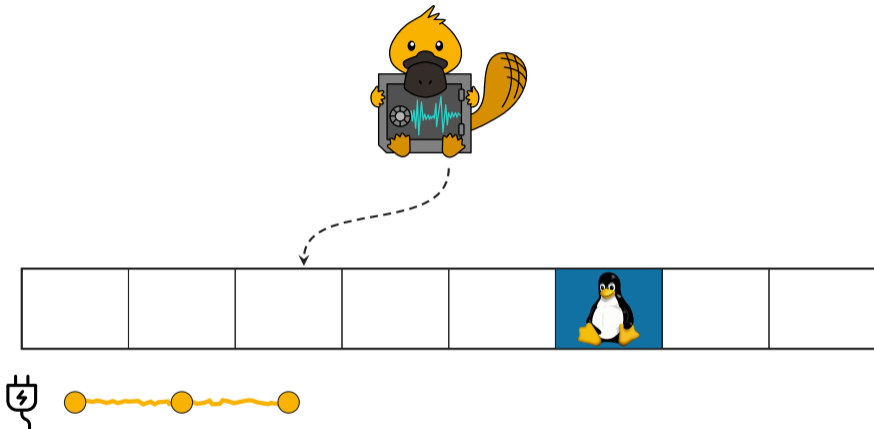
- Measure the **energy consumption** of **different operands**

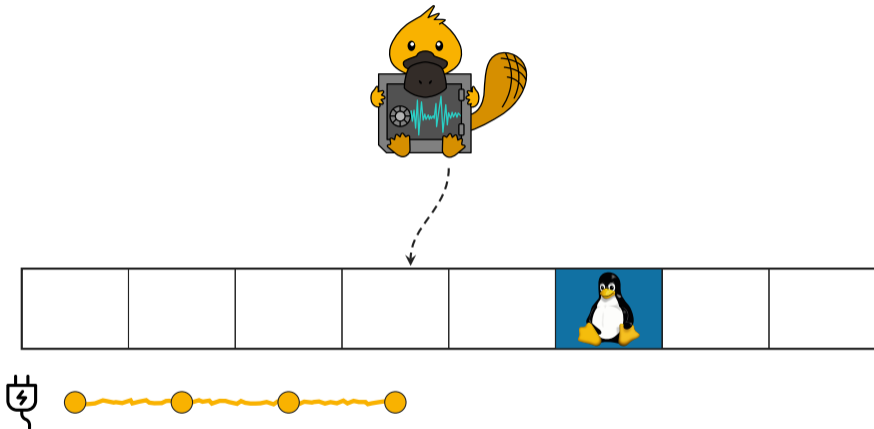


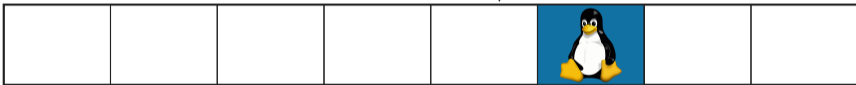


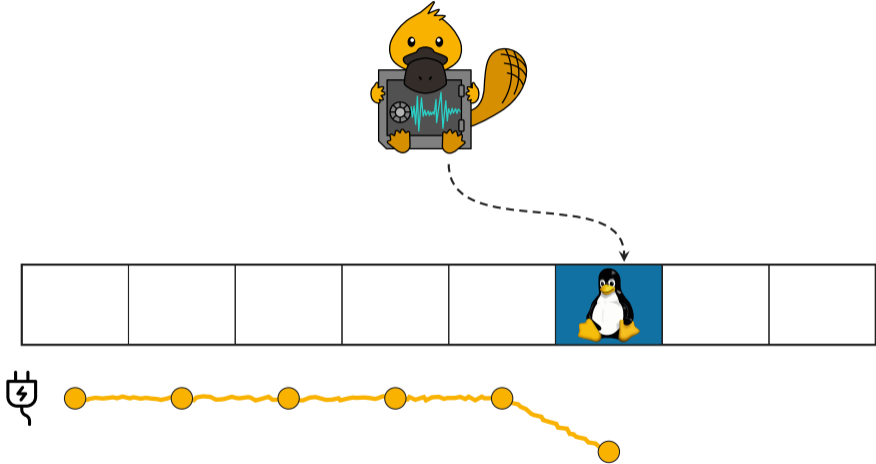


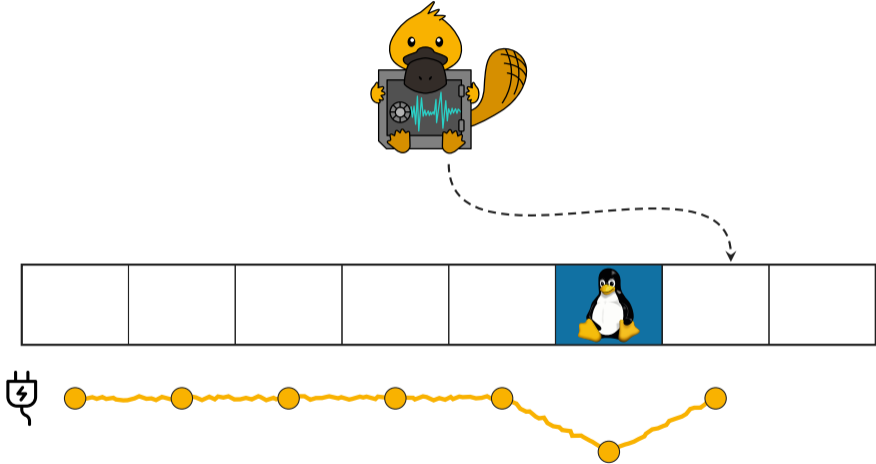


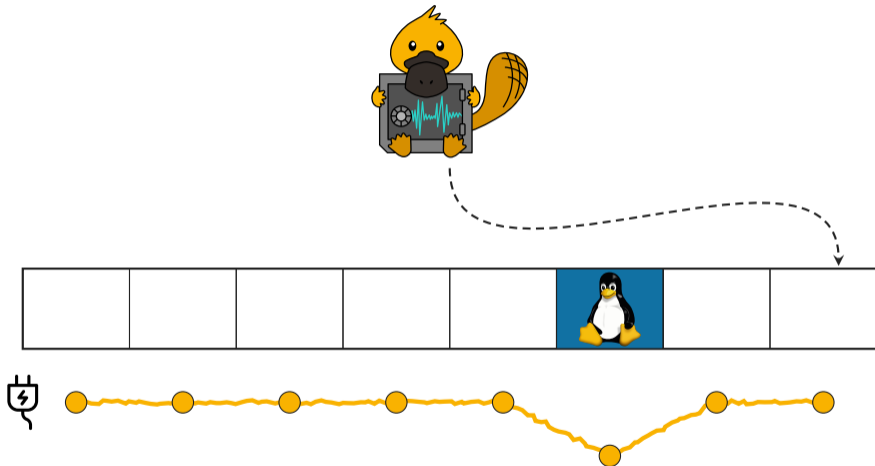


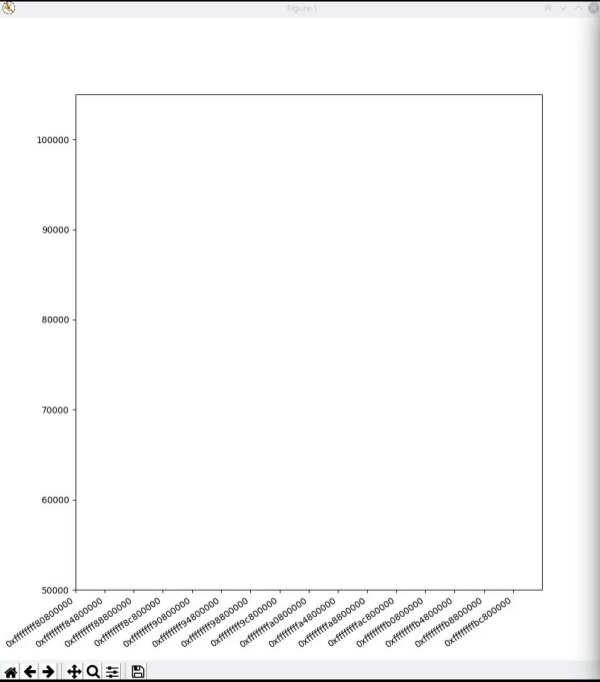












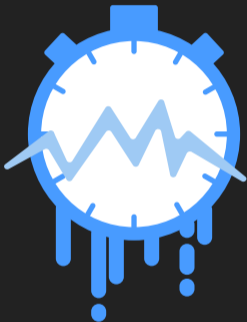
```
kaslr : zsh — Konsole
File Edit View Bookmarks Settings Help
michael@hp /tmp/kaslr %
```

```
→ ~      cat /sys/class/powercap/intel-rapl:0/intel-rapl:0:0/energy_uj  
90211251602
```

```
→ ~ sudo cat /sys/class/powercap/intel-rapl:0/intel-rapl:0:0/energy_uj  
90211251602
```

The end?

Hertzbleed²³



²Yingchen Wang, Riccardo Paccagnella, Elizabeth He, Hovav Shacham, Christopher W. Fletcher, and David Kohlbrenner. Hertzbleed: Turning Power Side-Channel Attacks Into Remote Timing Attacks on x86. In: USENIX Security. 2022.

³Chen Liu, Abhishek Chakraborty, Nikhil Chawla, and Neer Roggel. Frequency throttling side-channel attack. In: CCS. 2022.

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- In order to **save power**, you can ...

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Shut down resources

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Shut **down** resources



Reduce **voltage**

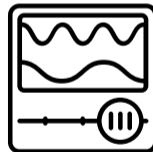
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Shut down resources



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Reduce **frequency**

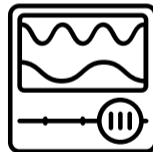
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Shut **down** resources



Reduce **voltage**



Reduce **frequency**







- Consumes **more** energy



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- Consumes **less** energy



- Consumes **more** energy
- **Reaches** power limit after some time



- Consumes **less** energy



- Consumes **more** energy
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- Consumes **less** energy
- **Never reaches** power limit



- Consumes **more** energy
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→ Slowdown



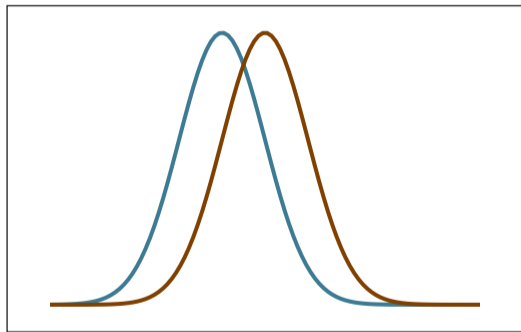
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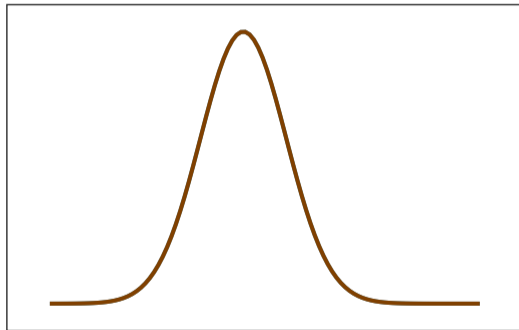
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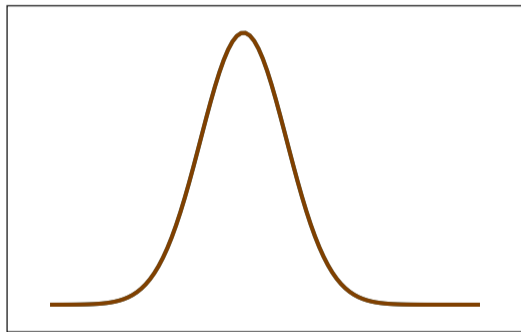
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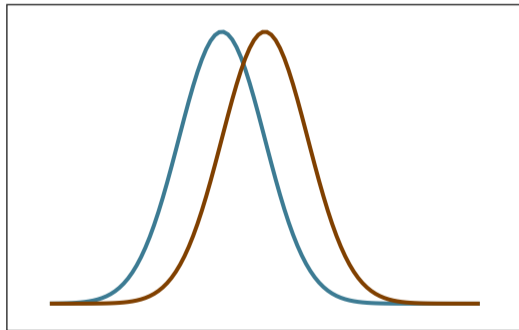
Energy



Time



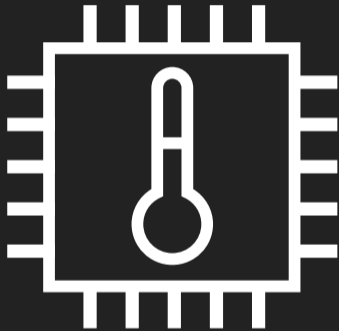
Energy



Time

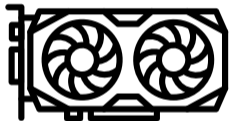


GPU Throttling⁴⁵

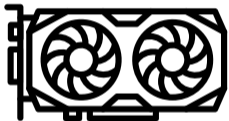


⁴Yingchen Wang, Riccardo Paccagnella, Alan Wandke, Zhao Gang, Grant Garrett-Grossman, Christopher W Fletcher, David Kohlbrenner, and Hovav Shacham. DVFS frequently leaks secrets: Hertzbleed attacks beyond SIKE, cryptography, and CPU-only data. In: S&P. 2023.

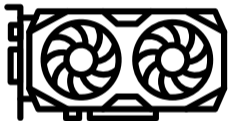
⁵Hritvik Taneja, Jason Kim, Jie Jeff Xu, Stephan van Schaik, Daniel Genkin, and Yuval Yarom. Hot Pixels: Frequency, Power, and Temperature Attacks on GPUs and ARM SoCs. In: USENIX Security.



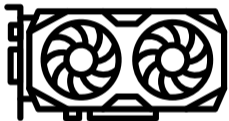
- Integrated GPUs **share** power limits with the CPU



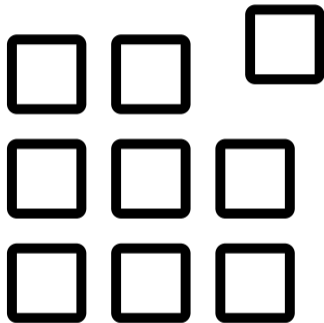
- **Integrated GPUs share** power limits with the CPU
→ **CPU throttling** indicates high GPU consumption



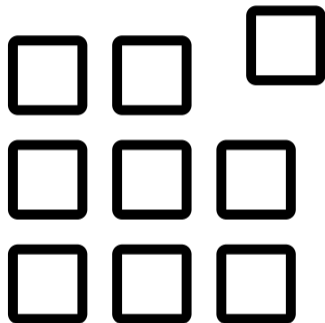
- **Integrated** GPUs **share** power limits with the CPU
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- **Dedicated** GPUs have power limits too



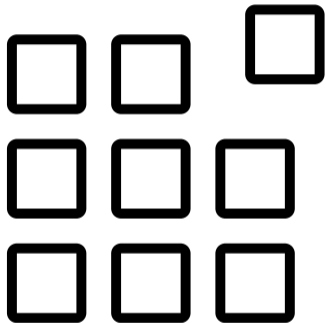
- **Integrated** GPUs **share** power limits with the CPU
 - **CPU throttling** indicates high GPU consumption
- **Dedicated** GPUs have power limits too
 - **Observable** by **timing** a GPU workload



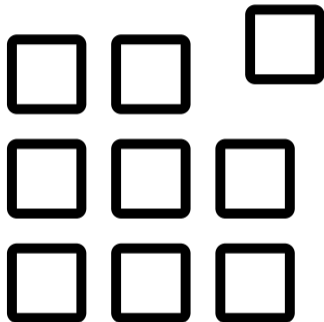
- What **secrets** are “*inside*” a GPU?



- What **secrets** are “*inside*” a GPU?
 - GPU renders windows and screen



- What **secrets** are “*inside*” a GPU?
 - GPU renders windows and screen
 - **Privacy** related information



- What **secrets** are “*inside*” a GPU?
 - GPU renders windows and screen
→ **Privacy** related information
- **Pixel** color **represents** the information



- Post-processing **without** revealing the pixels



- **Post-processing** **without** revealing the pixels
- Pixel value is the **data operand**



- **Post-processing** **without** revealing the pixels
- Pixel value is the **data operand**
- Distinguishable power consumption



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 - **Bright** pixel → **less** power



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- **Post-processing** **without** revealing the pixels
 - Pixel value is the **data operand**
 - Distinguishable power consumption
 - **Bright** pixel → **less** power
 - **Dark** pixel → **more** power
- **Measure timing and infer pixel value**

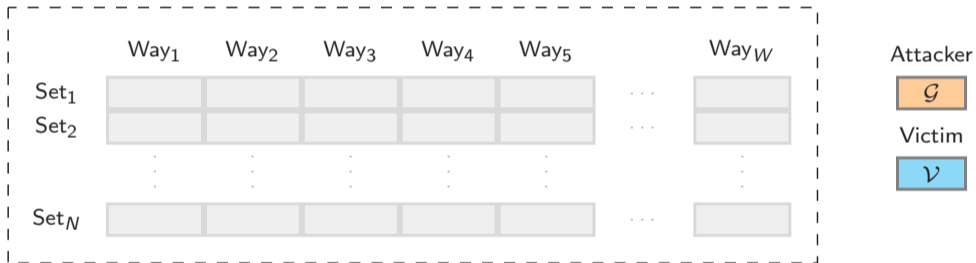


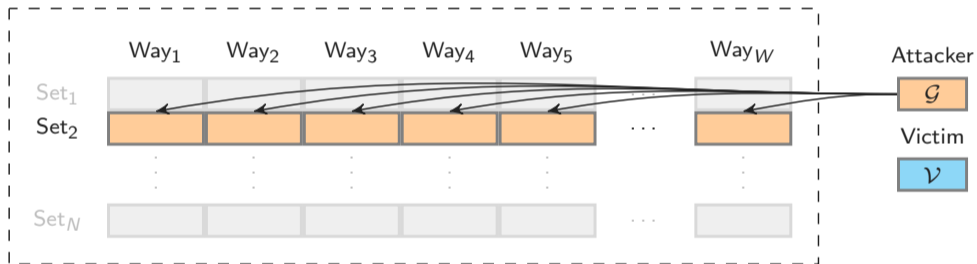
How can we **transform** power side channels towards a broader scope?

Collide+Power⁶

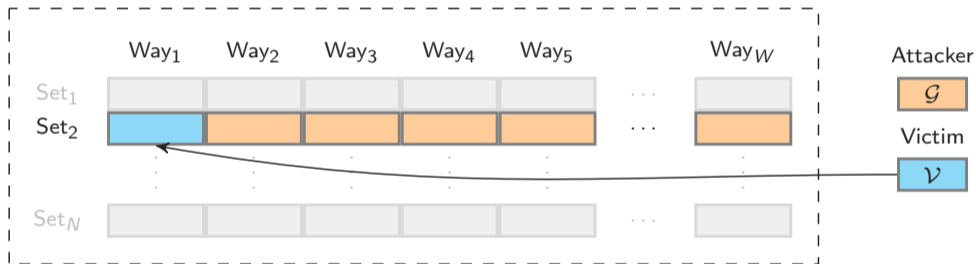


⁶Andreas Kogler, Jonas Juffinger, Lukas Giner, Lukas Gerlach, Martin Schwarzl, Michael Schwarz, Daniel Gruss, and Stefan Mangard. Collide+Power: Leaking Inaccessible Data with Software-based Power Side Channels. In: USENIX Security. 2023.





Collide+Power - Memory Subsystem







Hamming Weight: $hw(x)$



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Number of set bits



Hamming Weight: $hw(x)$

Number of set bits

$$hw(11_2) = 2$$



Hamming Weight: $hw(x)$

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Hamming Distance: $hd(x, y)$



Hamming Weight: $hw(x)$

Number of set bits

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Hamming Distance: $hd(x, y)$

Number of different bits



Hamming Weight: $hw(x)$

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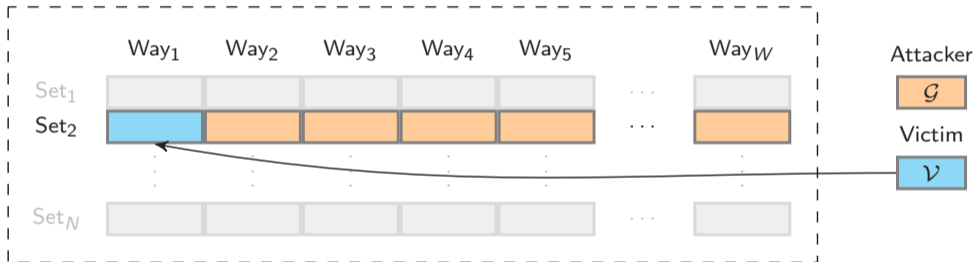


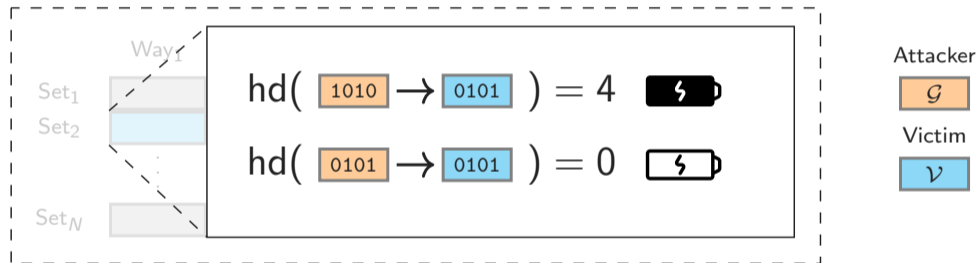
Hamming Distance: $hd(x, y)$

Number of different bits

$$hd(11_2, 01_2) = 1$$

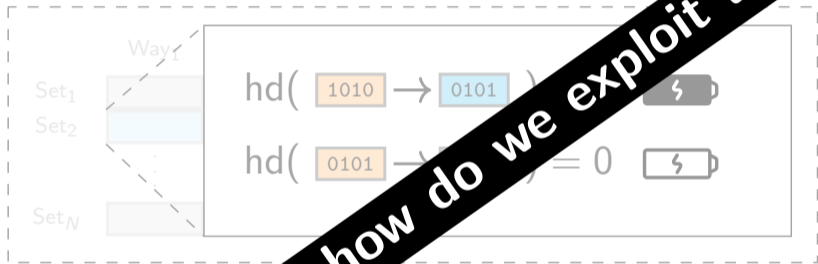
Collide+Power - Memory Subsystem







But how do we exploit this?



Attacker



Victim





$$\mathcal{P}(\mathcal{G}, \mathcal{V}) \approx \dots$$

$$\mathcal{P}(\mathcal{G}, \mathcal{V}) \approx \text{hd}(\mathcal{G}, \mathcal{V})$$

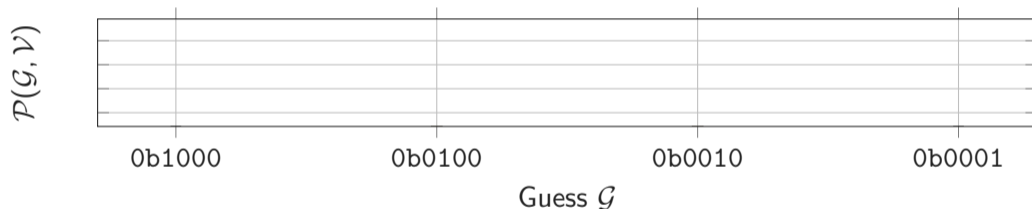


$$\mathcal{P}(\mathcal{G}, \mathcal{V}) \approx \text{hd}(\mathcal{G}, \mathcal{V})$$

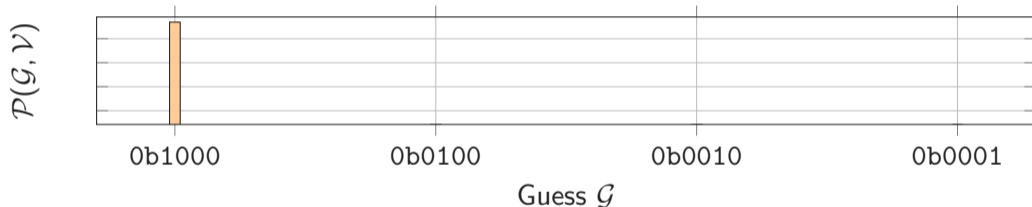
$$\underbrace{\mathcal{P}(\mathcal{G}, \mathcal{V})}_{\text{model}} \approx \text{hd}(\mathcal{G}, \mathcal{V})$$

$$\underbrace{\mathcal{P}(\mathcal{G}, \mathcal{V})}_{\text{model}} \approx \underbrace{\text{hd}(\mathcal{G}, \mathcal{V})}_{\text{signal}}$$

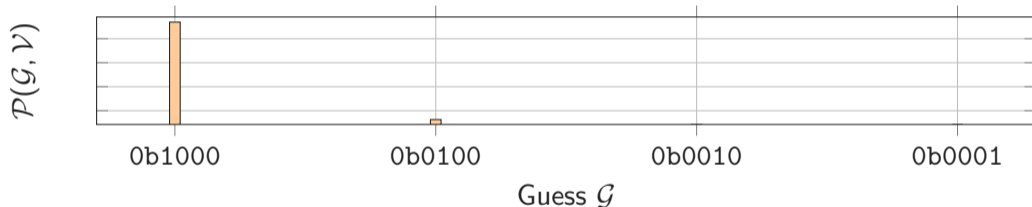
$$\mathcal{P}(\mathcal{G}, 0101_2) \approx \text{hd}(\mathcal{G}, 0101_2)$$



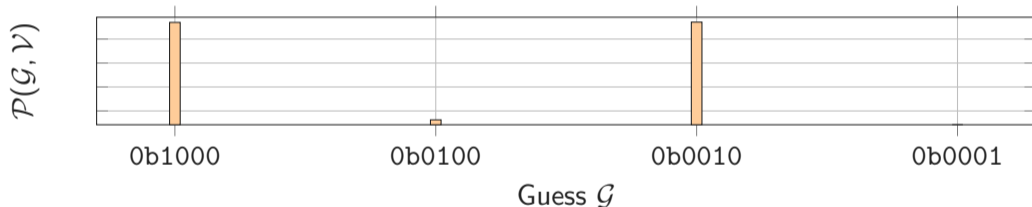
$$\mathcal{P}(1000_2, 0101_2) \approx \text{hd}(\mathbf{1}000_2, \mathbf{0}101_2) = 3$$



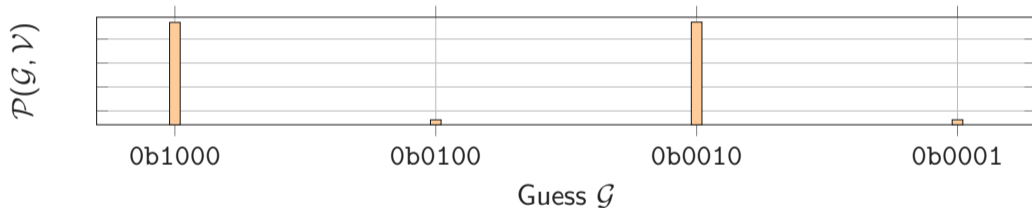
$$\mathcal{P}(0100_2, 0101_2) \approx \text{hd}(0\mathbf{1}00_2, 0\mathbf{1}01_2) = 1$$



$$\mathcal{P}(0010_2, 0101_2) \approx \text{hd}(00\mathbf{1}0_2, 01\mathbf{0}1_2) = 3$$

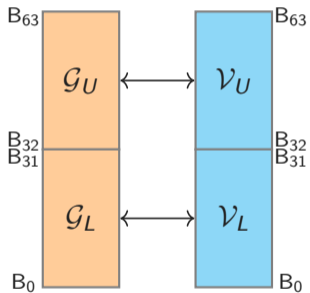


$$\mathcal{P}(0001_2, 0101_2) \approx \text{hd}(0001_2, 0101_2) = 1$$



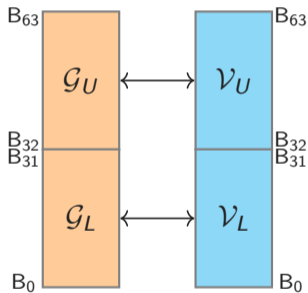


Aligned Leakage

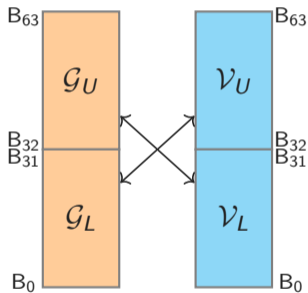




Aligned Leakage

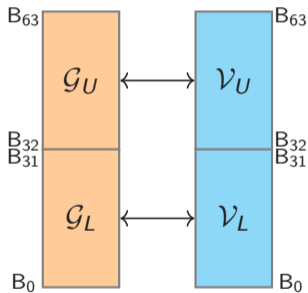


Cross Leakage

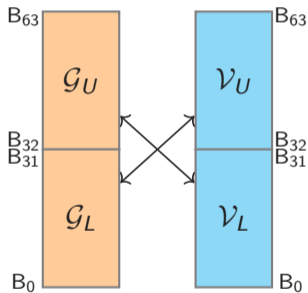




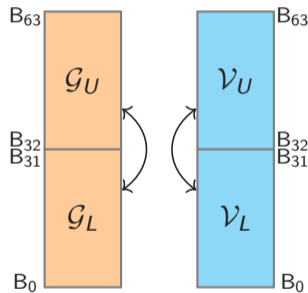
Aligned Leakage



Cross Leakage



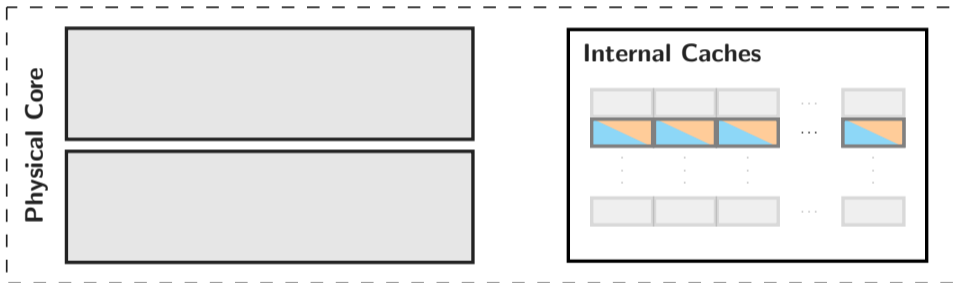
Self Leakage

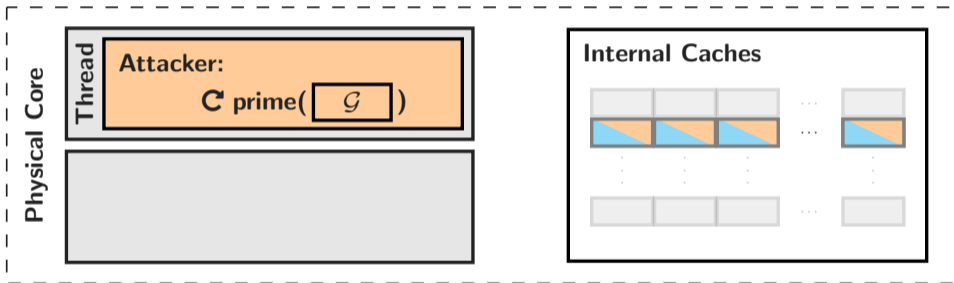


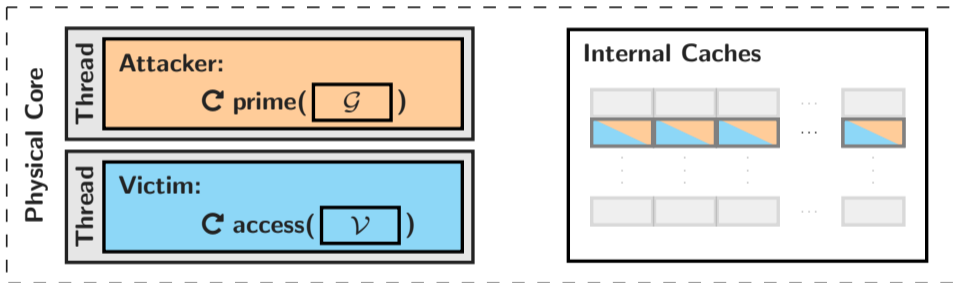
Inst.	Evict.	Effectiveness		Aligned Leakage		Cross Leakage		Self Leakage		Weights		
		$\hat{\rho}$ ·1	SNR_A ·10 ⁻³	$\text{hd}(v_L, g_L)$ a_0 in μW	$\text{hd}(v_U, g_U)$ a_1 in μW	$\text{hd}(v_L, g_U)$ c_0 in μW	$\text{hd}(v_U, g_L)$ c_1 in μW	$\text{hd}(v_L, v_U)$ s_0 in μW	$\text{hd}(g_L, g_U)$ s_1 in μW	$\text{hw}(v_L)$ w_1 in μW	$\text{hw}(g_L)$ w_2 in μW	$\text{hw}(g_U)$ w_3 in μW
Load	None	0.311	72.004	544.5	4.2	1.1	0.5	0.0	0.0	0.0	362.6	0.0
	L1	0.907	7.873	598.3	278.8	0.0	0.0	0.0	0.0	0.0	6124.4	2696.9
	L1+L2	0.822	5.632	339.3	141.7	106.6	40.9	0.0	0.0	0.0	3750.7	1435.0
Prefetch	None	0.003	0.000	0.0	0.0	0.0	0.0	0.0	0.0	0.0	1.7	2.8
	L1	0.370	11.365	18.0	18.0	0.1	0.1	0.0	0.0	0.0	454.1	455.5
	L1+L2	0.300	5.294	10.9	10.9	40.9	43.0	0.0	0.0	0.0	334.0	332.5
Store	None	0.003	0.000	0.0	0.0	0.0	3.1	0.0	0.0	0.0	7.0	0.0
	L1	0.241	3.876	63.3	74.5	4.9	9.6	0.0	0.0	0.0	204.6	303.2
	L1+L2	0.450	6.457	133.7	169.0	84.7	86.2	0.0	0.0	0.0	347.1	1130.5

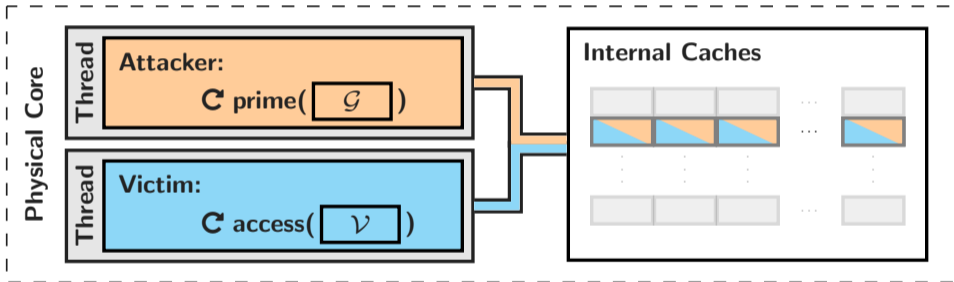
Do not start reading this!

Generic Attacks

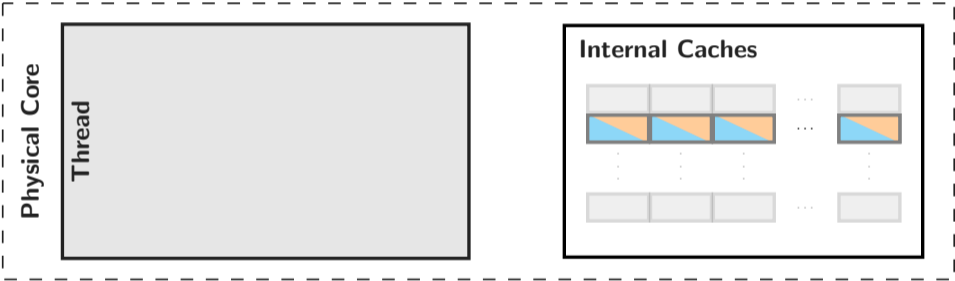




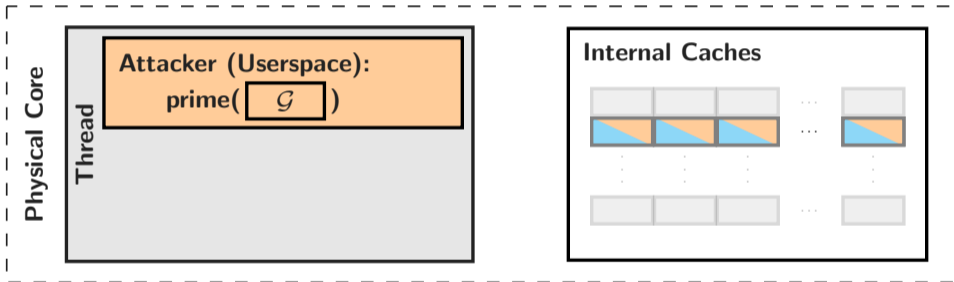




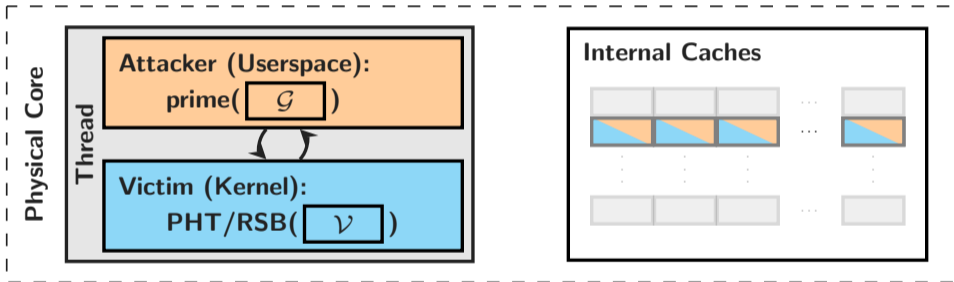
Meltdown-style Attack



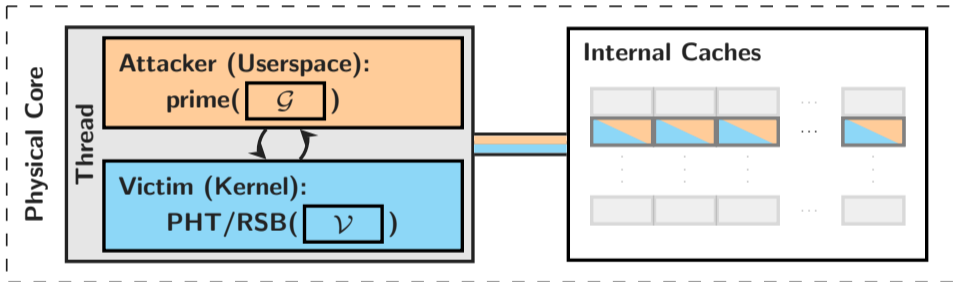
Meltdown-style Attack



Meltdown-style Attack



Meltdown-style Attack

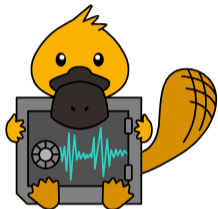


This must be slow?

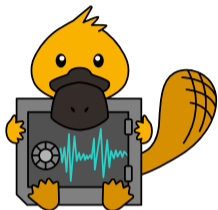
NO!

It is **EXTREMELY** slow!⁷

⁷With the current state-of-the-art.



- **MDS-style:**
4.82 bit/h



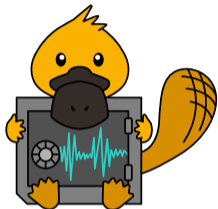
- **MDS-style:**
4.82 bit/h
- **Meltdown-style (RSB):**
0.84 bit/h



- **MDS-style:**
4.82 bit/h
- **Meltdown-style (RSB):**
0.84 bit/h



- **MDS-style:**
0.065 to 0.68 bit/h



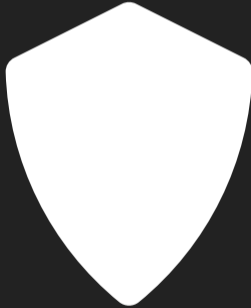
- **MDS-style:**
4.82 bit/h
- **Meltdown-style (RSB):**
0.84 bit/h



- **MDS-style:**
0.065 to 0.68 bit/h
- **Meltdown-style estimate (PHT):**
99.95 days/bit to 2.86 years/bit

DEMO

Mitigations





- **Preventing data collisions:**
 - Redesign of the **complete** shared data path
 - Costly to deploy
 - **Missed** components re-enable Collide+Power



- **Preventing observable power consumption:**
 - **Restricting** all direct power interfaces
 - **Mitigating** Hertzbleed is **challenging**
 - Thermal and power management is required
- **Collide+Power** is slow but **unmitigated** on modern CPUs!

- **Unrestricted** power interfaces are a **threat** for system security





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- **Indirect interfaces** still expose **exploitable** information



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- **Unrestricted** power interfaces are a **threat** for system security
- **Indirect interfaces** still expose **exploitable** information
- **Software-based power side channels** can leak **arbitrary** data
- **Many more details** in the papers

<https://collidepower.com>

<https://hertzbleed.com>

<https://platypusattack.com/>