black hat ASIA 2019

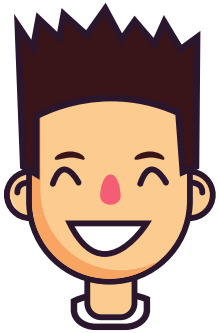
NetSpectre

A Truly Remote Spectre Variant

Michael Schwarz @misc0110

Martin Schwarzl @marv0x90

Who am I?



Michael Schwarz

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Martin Schwarzl

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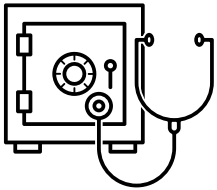
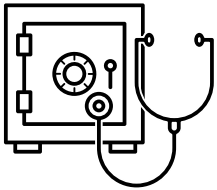
m.schwarzl@student.tugraz.at

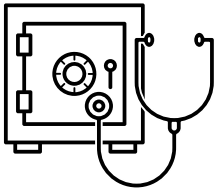
- Bug-free software does not mean safe execution



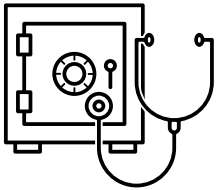
Side-Channel Attacks

- Bug-free software does not mean safe execution
- Information leaks due to underlying hardware





- Bug-free software does not mean safe execution
- Information leaks due to underlying hardware
- Exploit leakage through side-effects



- Bug-free software does not mean safe execution
- Information leaks due to underlying hardware
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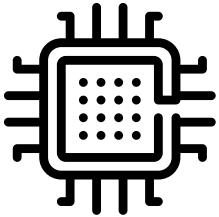
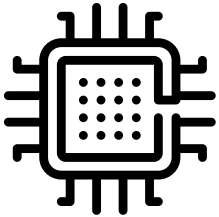
Power consumption

Execution time

CPU caches



- Instruction Set Architecture (ISA) is an abstract model of a computer (x86, ARMv8, SPARC, …)



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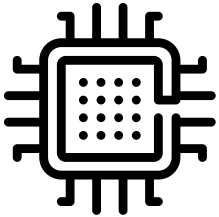

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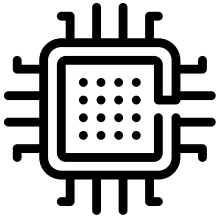
- Microarchitecture is an ISA implementation



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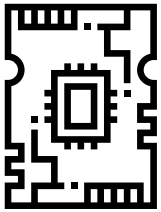
Microarchitectural Components



- Modern CPUs contain multiple microarchitectural elements

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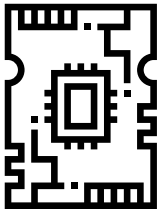
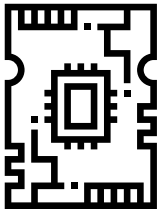


Caches and buffers

Predictors



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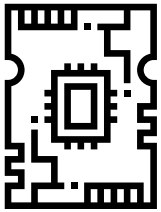
Caches and buffers

Predictors

- Transparent for the programmer



- Modern CPUs contain multiple microarchitectural elements

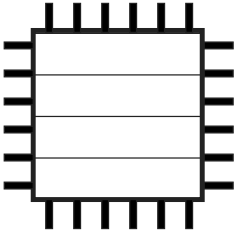
Caches and buffers

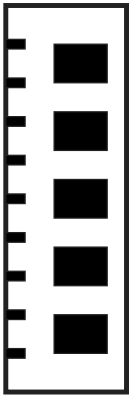
Predictors

- Transparent for the programmer
- Timing optimizations → side-channel leakage

Let’s have a deeper look at the cache

```
printf("%d", i);
printf("%d", i);
```





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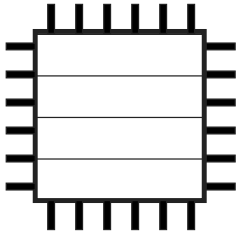

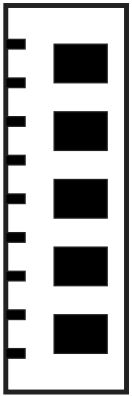

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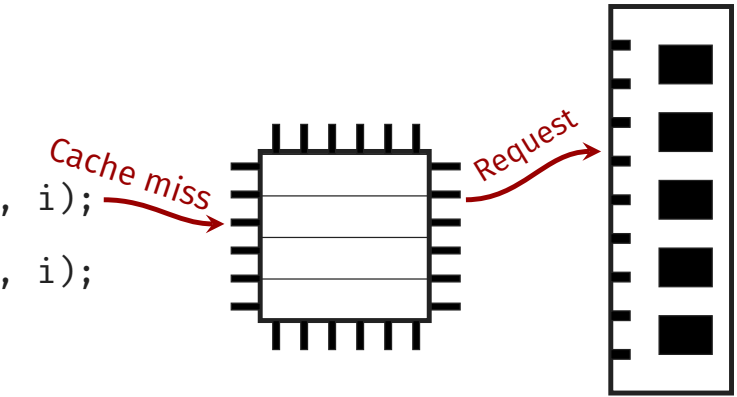

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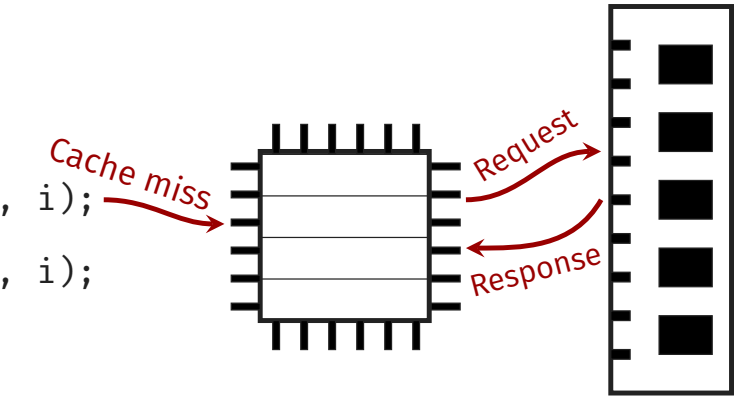
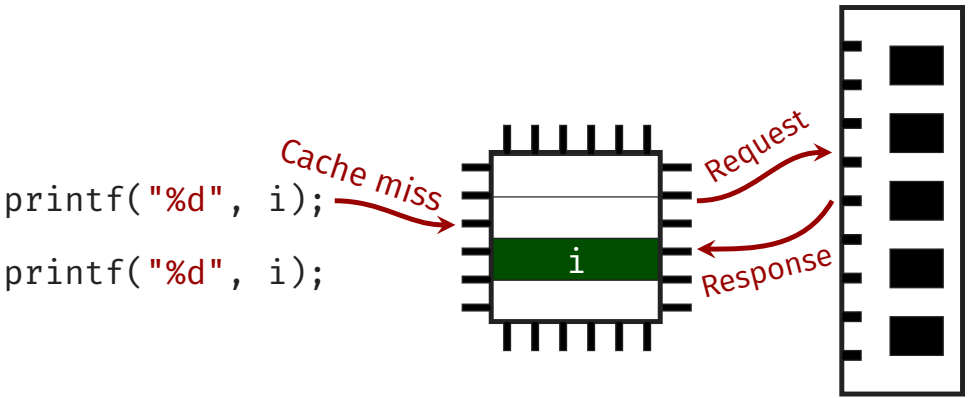
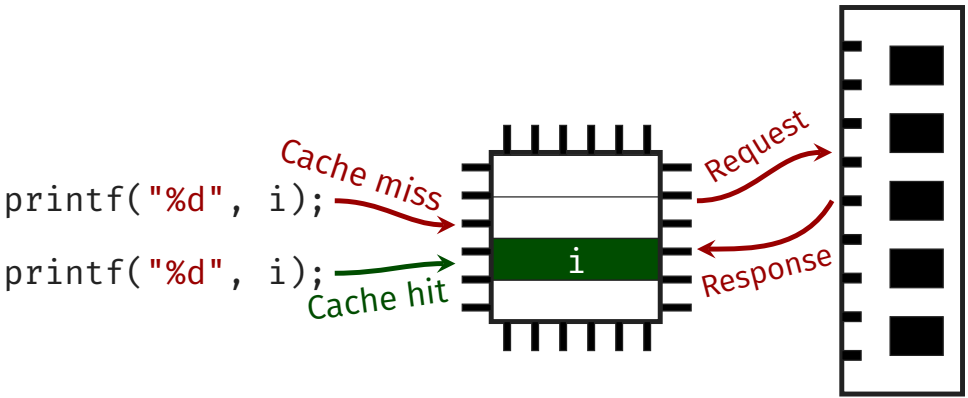



printf("%d", i);
printf("%d", i);
Cache miss
i
Request
Response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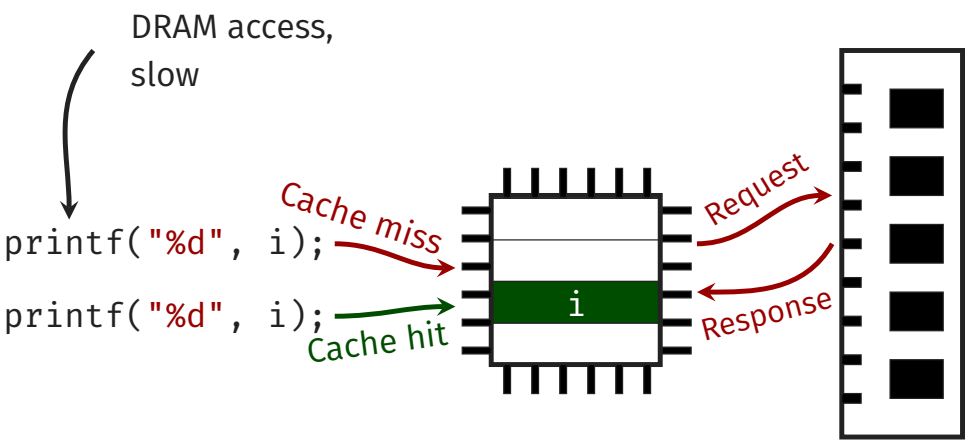
DRAM access,
slow
printf("%d", i);
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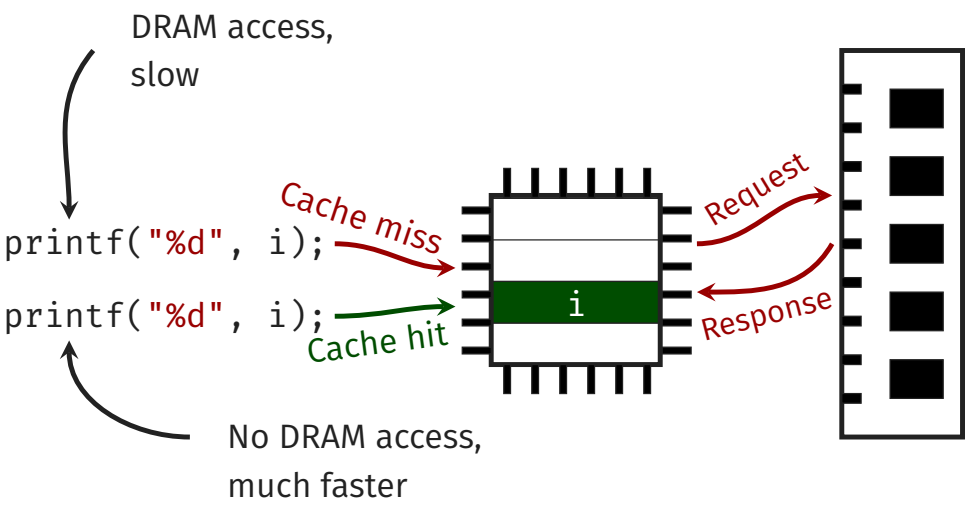
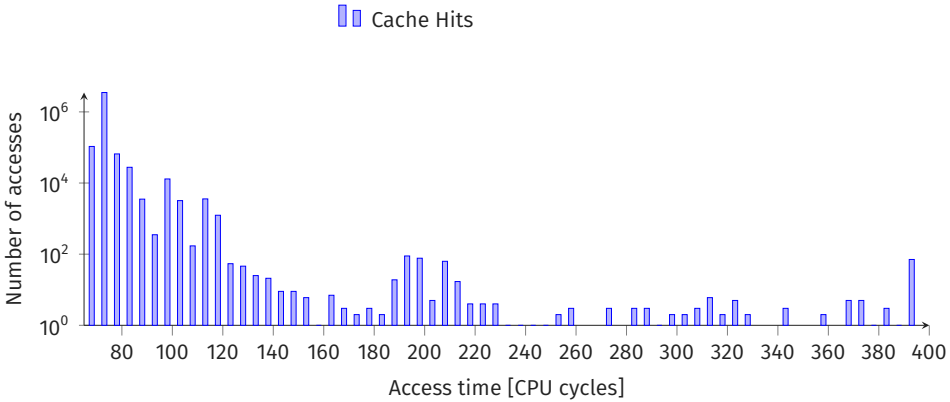
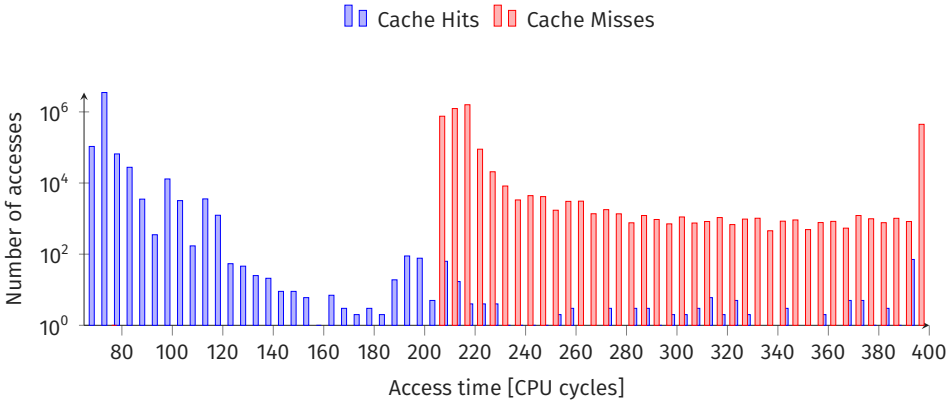
Cache miss
Cache hit
i
Request
Response

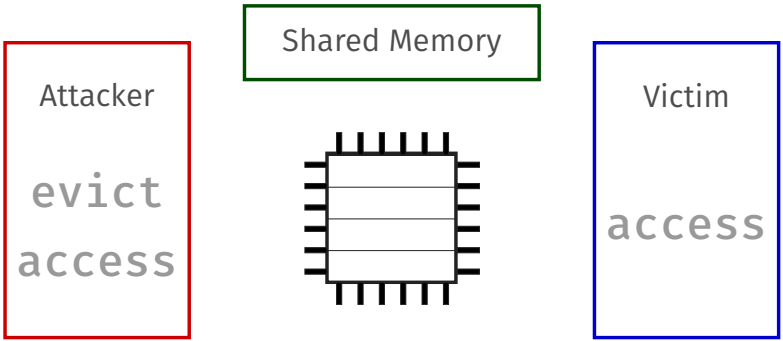

DRAM access,
slow
printf("%d", i);
printf("%d", i);
Cache miss
Cache hit
i
Request
Response
No DRAM access,
much faster

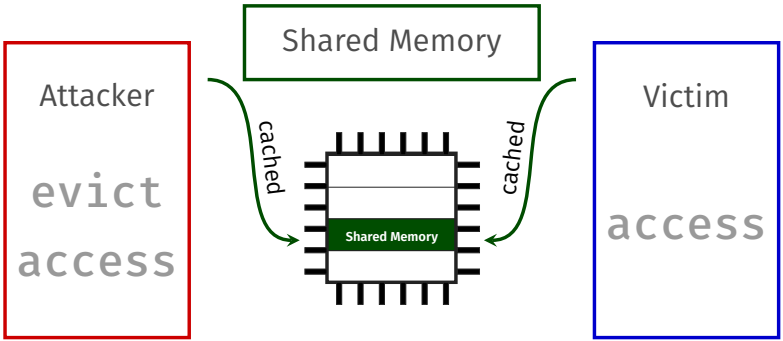
Caching speeds up Memory Accesses

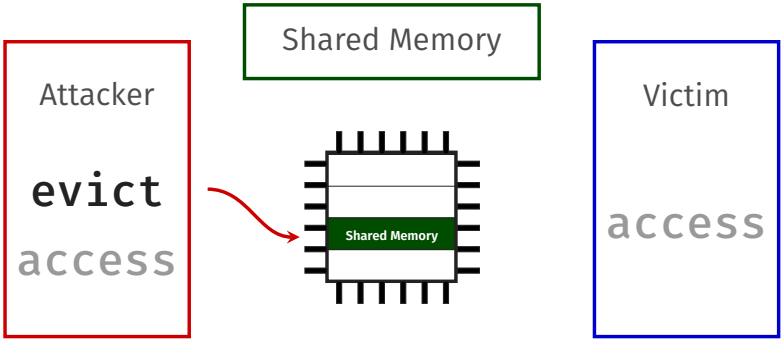


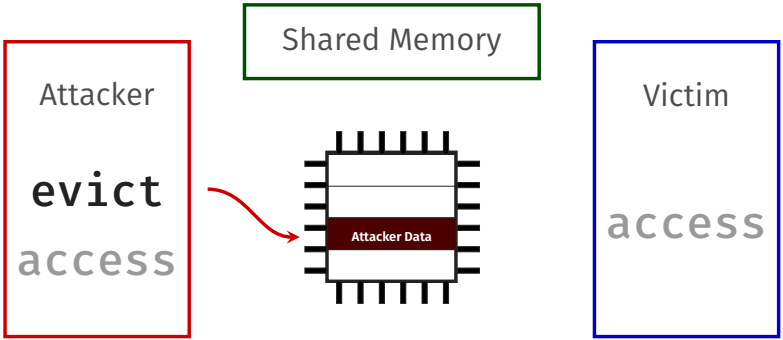
Caching speeds up Memory Accesses

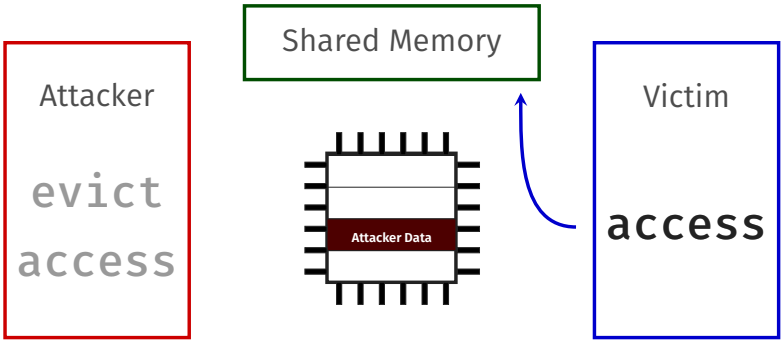


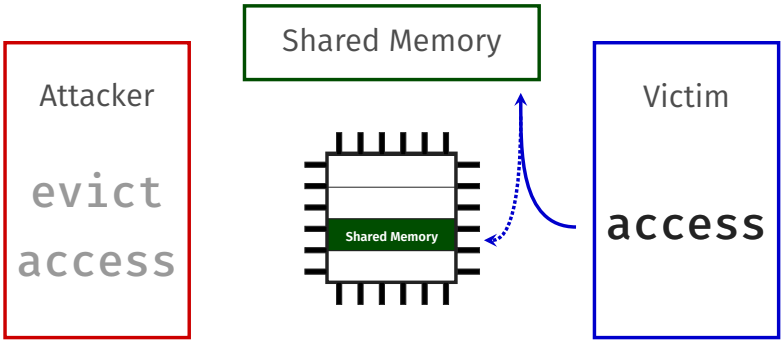

Shared Memory
Attacker
evict
access
Victim
access

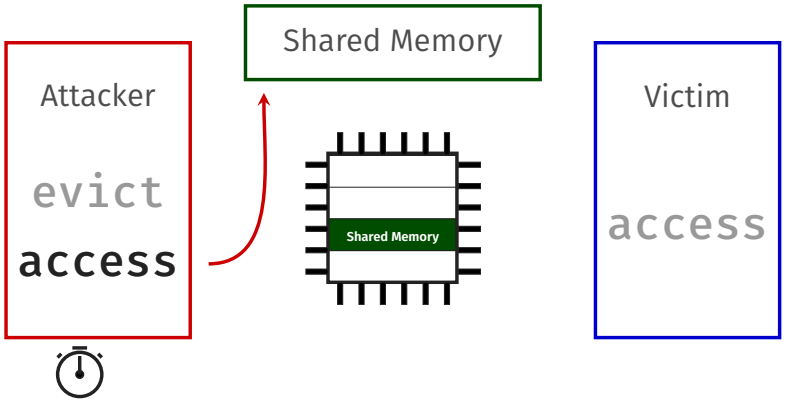

Shared Memory
Attacker
evict
access
cached
cached
Shared Memory
Victim
access

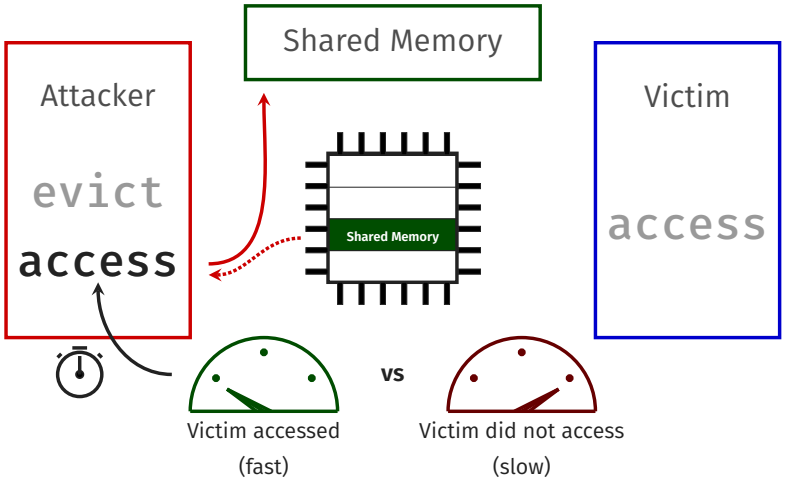

Shared Memory
Attacker
evict
access
Shared Memory
Victim
access


Shared Memory
Attacker
evict
access
Attacker Data
Victim
access


Shared Memory
Attacker
evict
access
Attacker Data
Victim
access


Shared Memory
Attacker
evict
access
Shared Memory
Victim
access


Shared Memory
Attacker
evict
access
Shared Memory
Victim
access


Shared Memory
Attacker
evict
access
Shared Memory
Victim
access
vs
Victim accessed
(fast)
Victim did not access
(slow)

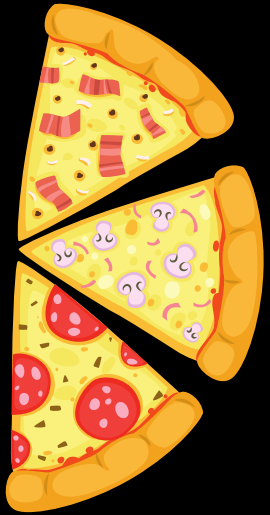
Speculative execution

- CPU tries to predict the future (branch predictor), …
  - …based on events learned in the past
- Speculative execution of instructions
- If the prediction was correct, …
  - …very fast
  - otherwise: Discard results
- Measurable side-effects

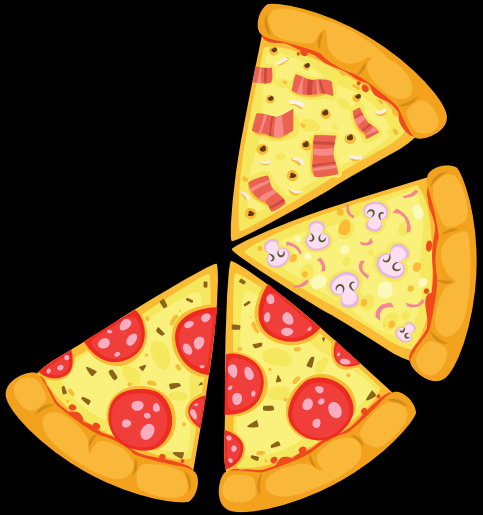

PIZZA
SPECIAL RECIPES

Prosciutto

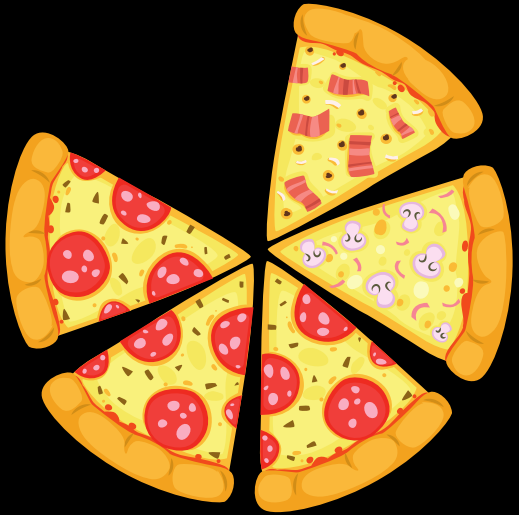
Funghi



Diavolo



Diavolo



Diavolo

Diavolo


»A table for 6 please«

Speculative Cooking


»A table for 6 please«


PIZZA
SPECIAL RECIPES


PIZZA
SPECIAL RECIPES

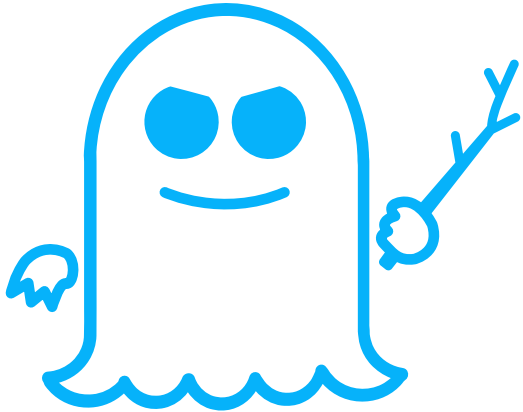

Pizza


PIZZA
SPECIAL RECIPES

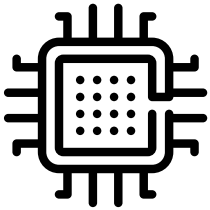

Pizza


PIZZA
SPECIAL RECIPES

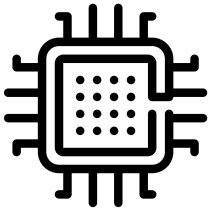

Pizza



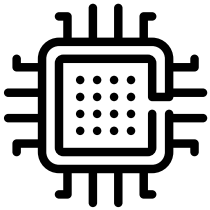
SPECTRE



- On Intel and AMD CPUs



- On Intel and AMD CPUs
- Some ARMs (Cortex R and Cortex A) are also affected



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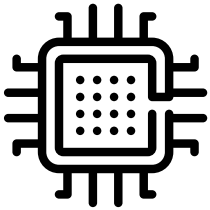
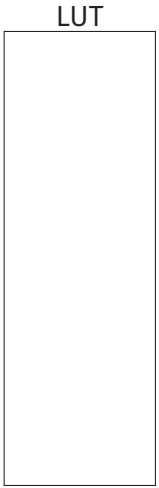


- On Intel and AMD CPUs
- Some ARMs (Cortex R and Cortex A) are also affected
- Common cause: speculative execution of branches
- Speculative execution leaves microarchitectural traces which leak secret




```
index = 0;

char* data = "textKEY";

if (index < 4)
```

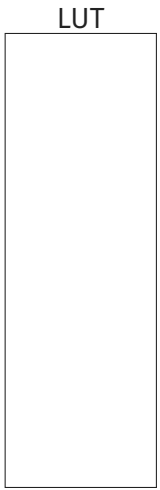
then

Prediction

else

```
LUT[data[index] * 4096]
```

0

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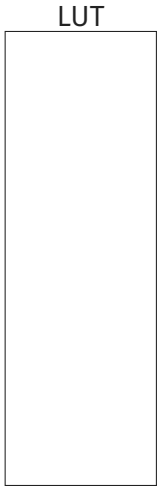


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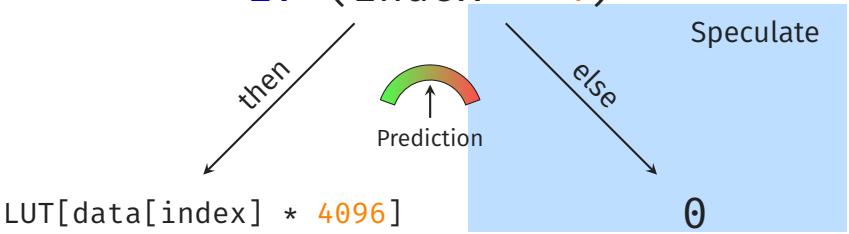

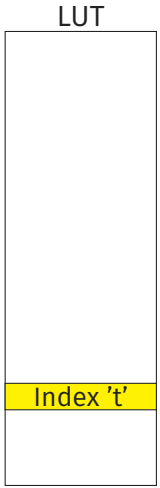


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index = 0;

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if (index < 4)
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Execute

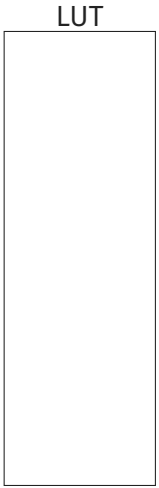
then

Prediction

else

```
LUT[data[index] * 4096]
```

0




```
index = 1;

char* data = "textKEY";

if (index < 4)
```

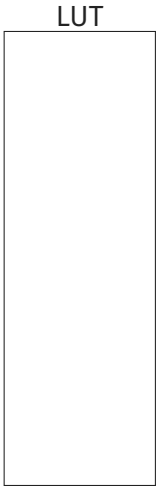
then

Prediction

else

```
LUT[data[index] * 4096]
```

```
0
```

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index = 1;

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if (index < 4)
```

then

Prediction

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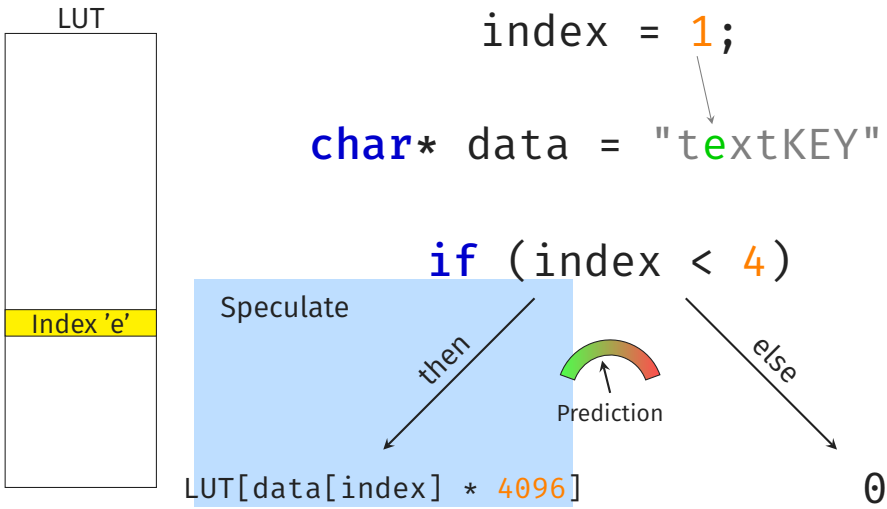
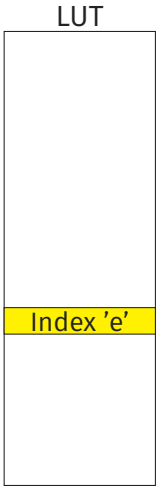
```
LUT[data[index] * 4096]
```

0


LUT
Index 'e'
index = 1;
char* data = "textKEY";
if (index < 4)
Speculate
then
else
Prediction
LUT[data[index] * 4096]
0




```
index = 1;

char* data = "textKEY";

if (index < 4)
```

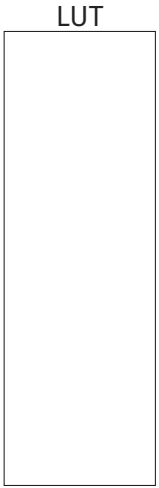
then

Prediction

else

```
LUT[data[index] * 4096]
```

0




```
index = 2;

char* data = "textKEY";

if (index < 4)
```

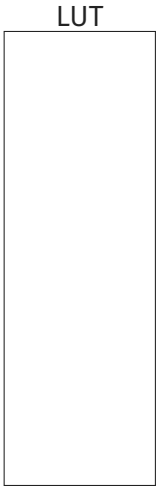
then

Prediction

else

```
LUT[data[index] * 4096]
```

```
0
```




```
index = 2;

char* data = "textKEY";

if (index < 4)
```

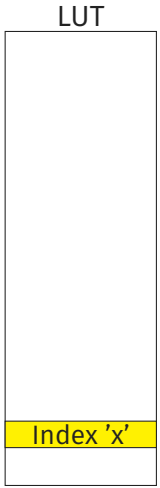
then

else

Prediction

```
LUT[data[index] * 4096]
```

```
0
```




```
index = 2;

char* data = "textKEY";

if (index < 4)
```

Speculate

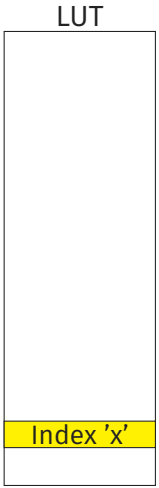
then

Prediction

else

```
LUT[data[index] * 4096]
```

0




```
index = 2;

char* data = "textKEY";

if (index < 4)
```

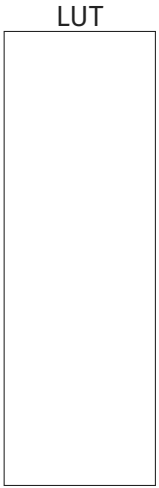
then

Prediction

else

```
LUT[data[index] * 4096]

0
```




```
index = 3;

char* data = "textKEY";

if (index < 4)
```

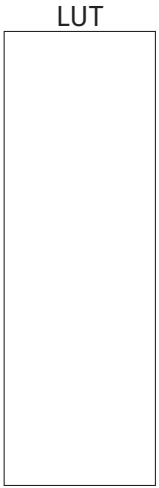
then

Prediction

else

```
LUT[data[index] * 4096]
```

0

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index = 3;

char* data = "textKEY";

if (index < 4)
```

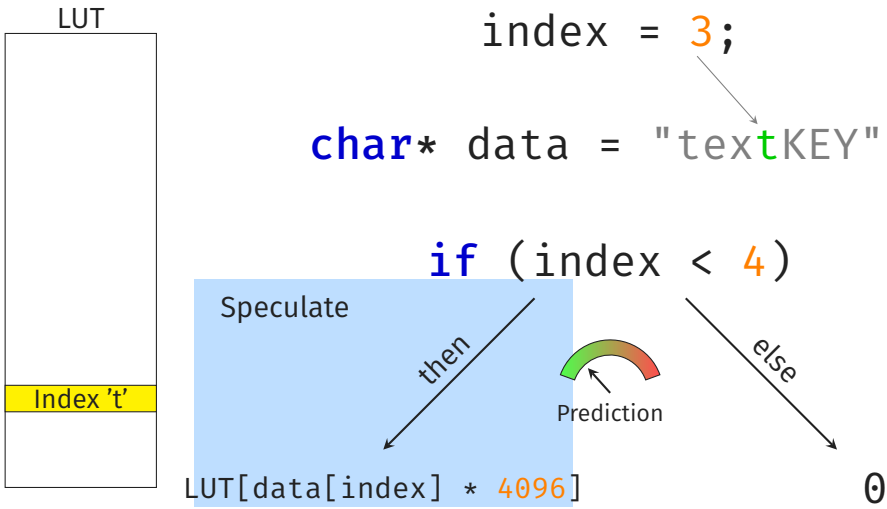
then

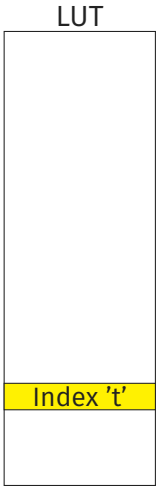
Prediction

else

```
LUT[data[index] * 4096]
```

```
0
```


LUT
Index 't'
index = 3;
char* data = "textKEY";
if (index < 4)
Speculate
then
else
Prediction
LUT[data[index] * 4096]
0




```
index = 3;

char* data = "textKEY";

if (index < 4)
```

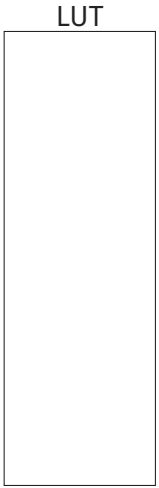
then

Prediction

else

```
LUT[data[index] * 4096]
```

0

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Prediction

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LUT[data[index] * 4096]
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```
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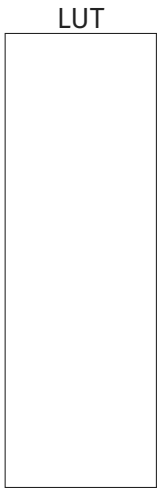


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```

then

Prediction

else

```
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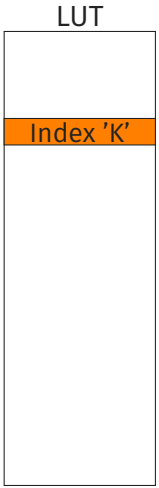


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index = 4;

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Speculate

then

else

Prediction

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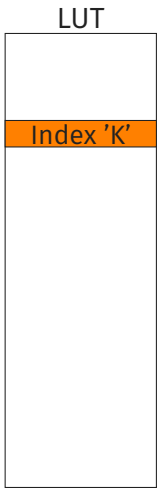



```
index = 4;

char* data = "textKEY";

if (index < 4)
```

then

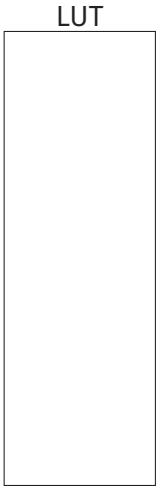
else

Prediction

Execute

```
LUT[data[index] * 4096]
```

0




```
index = 5;

char* data = "textKEY";

if (index < 4)
```

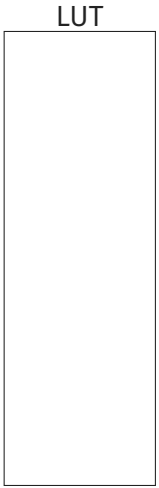
then

Prediction

else

```
LUT[data[index] * 4096]
```

0




```
index = 5;

char* data = "textKEY";

if (index < 4)
```

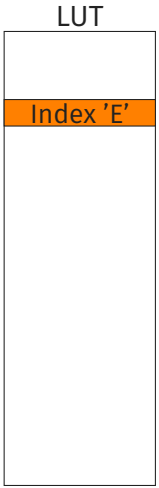
then

Prediction

else

```
LUT[data[index] * 4096]

0
```




```
index = 5;

char* data = "textKEY";

if (index < 4)
```

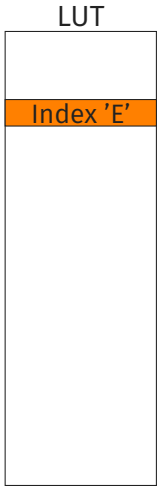
Speculate

then

else


```
LUT[data[index] * 4096]
```

0




```
index = 5;

char* data = "textKEY";

if (index < 4)
```

then

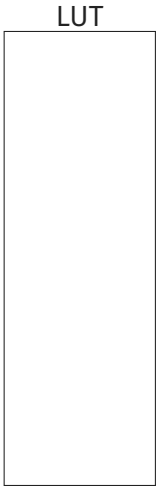
Prediction

else

Execute

0

```
LUT[data[index] * 4096]
```




```
index = 6;

char* data = "textKEY";

if (index < 4)
```

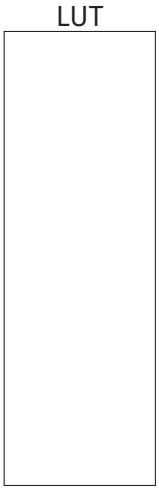
then

Prediction

else

```
LUT[data[index] * 4096]
```

```
0
```




```
index = 6;

char* data = "textKEY";

if (index < 4)
```

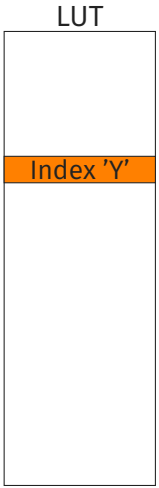
then

Prediction

else

```
LUT[data[index] * 4096]
```

0




```
index = 6;

char* data = "textKEY";

if (index < 4)
```

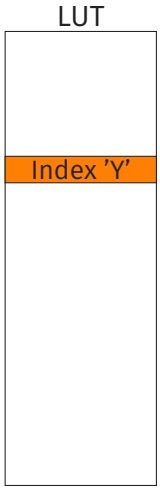
Speculate

then

else


```
LUT[data[index] * 4096]
```

```
0
```




```
index = 6;

char* data = "textKEY";

if (index < 4)
```

then

Prediction

else

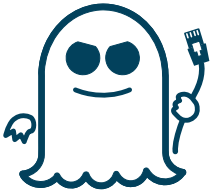
Execute

0

```
LUT[data[index] * 4096]
```

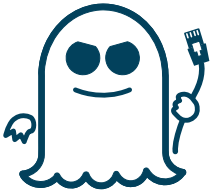
NetSpectre: A Remote Spectre Variant

The goal



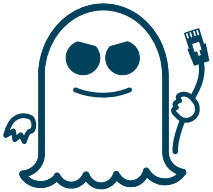
We want to build a Spectre attack which...

The goal



We want to build a Spectre attack which...

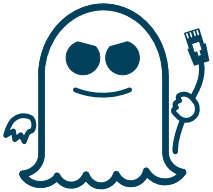
- is capable of leaking secrets from a remote system



We want to build a Spectre attack which...

- is capable of leaking secrets from a remote system
- has neither physical access nor code execution on system

The goal



We want to build a Spectre attack which...

- is capable of leaking secrets from a remote system
- has neither physical access nor code execution on system
- does not rely on software vulnerabilities

CVSS v3 for CVE-2017-5753 (Spectre)

Attack Vector

Network	Adjacent Network	**Local**	Physical

CVSS v3 for CVE-2017-5753 (Spectre)

Attack Vector

Network	Adjacent Network	**Local**	Physical

Attack Complexity

Low	**High**

CVSS v3 for CVE-2017-5753 (Spectre)

Attack Vector

Network	Adjacent Network	**Local**	Physical

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Low	**High**

Privilege Required

None	**Low**	High

CVSS v3 for CVE-2017-5753 (Spectre)

Attack Vector

Network	Adjacent Network	**Local**	Physical

Attack Complexity

Low	**High**

Privilege Required

None	**Low**	High

User Interaction

None	Required

Spectre without code execution is complicated

Spectre without code execution is complicated

- Which branch can be exploited

Spectre without code execution is complicated

- Which branch can be exploited
- Cannot observe the cache state

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- Spectre gadgets will be different

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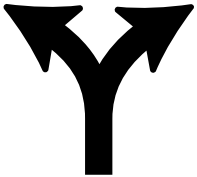
- No timing measurement on the attacked system

Spectre without code execution is complicated

- Which branch can be exploited
- Cannot observe the cache state
- Spectre gadgets will be different
- No timing measurement on the attacked system
- How to select the data to leak



- No code can be injected

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- Branches in API can be mistrained remotely

- No code can be injected
- Public interface (API) accessing data
- Branches in API can be mistrained remotely
- Attacker only calls the API via network requests

```
def check_user_privileges(user_id):
  [...]
  if user_id < len(users):
    if test_bit(privileges, user_id) == True:
      admin = True

  return SUCCESS
```

API Example

```
def check_user_privileges(user_id):
  [...]
  if user_id < len(users):
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Bounds check

API Example

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def check_user_privileges(user_id):
  [...]
  if user_id < len(users):
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```

Bounds check

Speculative out-of-bounds read

API Example

```
def is_admin():
  return admin
```

API Example

```
def is_admin():
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API Example

```
def is_admin():
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```

- If bit in array was set → `admin` is cached

```
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```

- If bit in array was set → `admin` is cached
- If bit was not set → `admin` is not cached

```
def is_admin():
  return admin
```

- If bit in array was set → `admin` is cached
- If bit was not set → `admin` is not cached
- Observe cache state via function execution time

- Cannot measure time directly on the attacked system

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- Network latency depends on API execution time

Timing Measurement

- Cannot measure time directly on the attacked system
- Network latency depends on API execution time

→ Measure the network roundtrip time

Timing Measurement

- Cannot measure time directly on the attacked system
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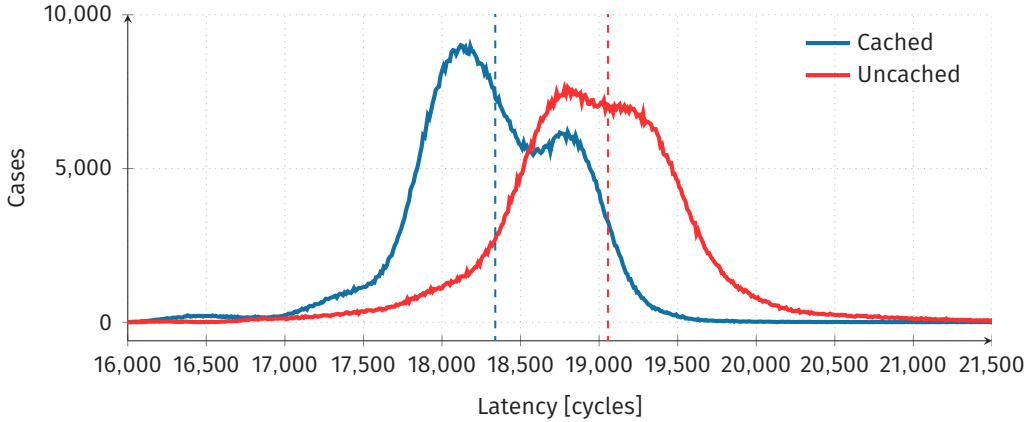
→ Measure the network roundtrip time

- Reveals whether the variable is cached


10,000
5,000
0
Cases
Cached
Uncached
16,000
16,500
17,000
17,500
18,000
18,500
19,000
19,500
20,000
20,500
21,000
21,500
Latency [cycles]

- After measuring variable is always cached

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- How do we evict the variable?

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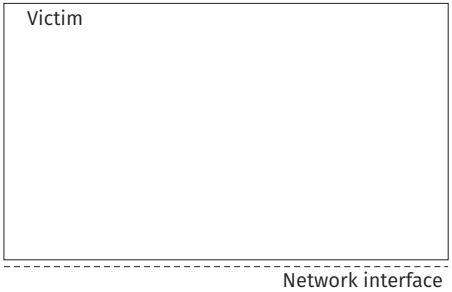
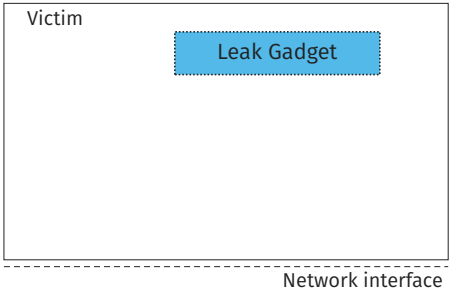
- How do we evict the variable?
- Constantly evict the cache via a file download

- After measuring variable is always cached
- How do we evict the variable?
- Constantly evict the cache via a file download
- Thrash+Reload $\rightarrow$ crude form of Evict+Reload

NetSpectre - The Big Picture

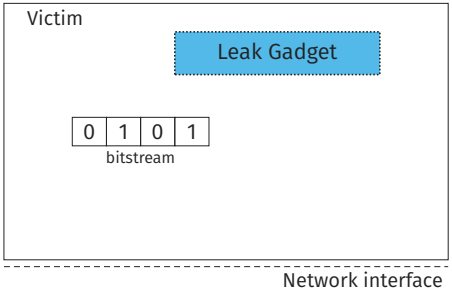


NetSpectre - The Big Picture




```
if (x < bitstream_length)
   if(bitstream[x])
      flag = true
```

NetSpectre - The Big Picture

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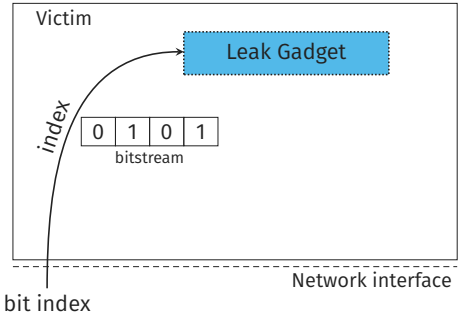


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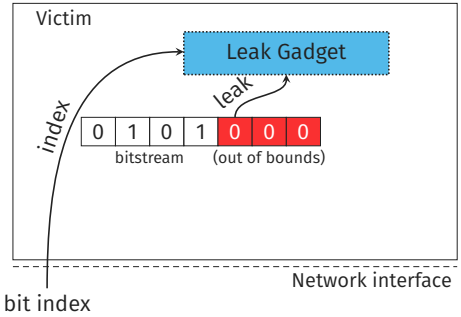
NetSpectre - The Big Picture

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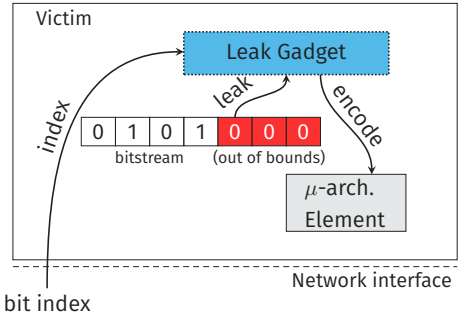
```

NetSpectre - The Big Picture

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if (x < bitstream_length)
   if(bitstream[x])
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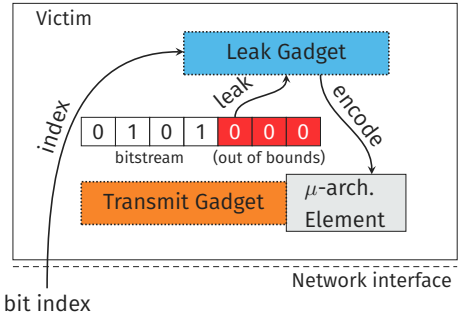


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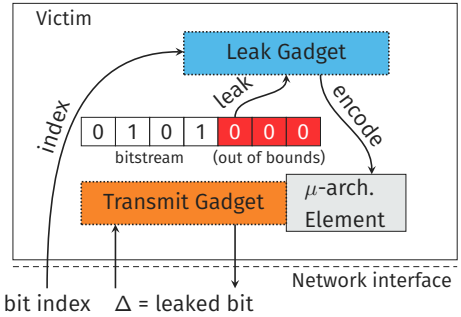


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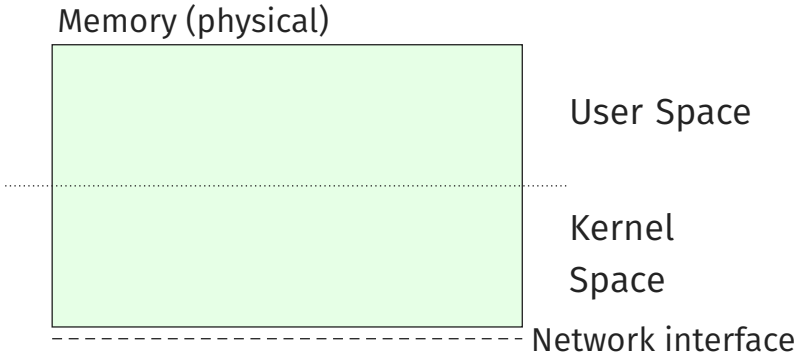
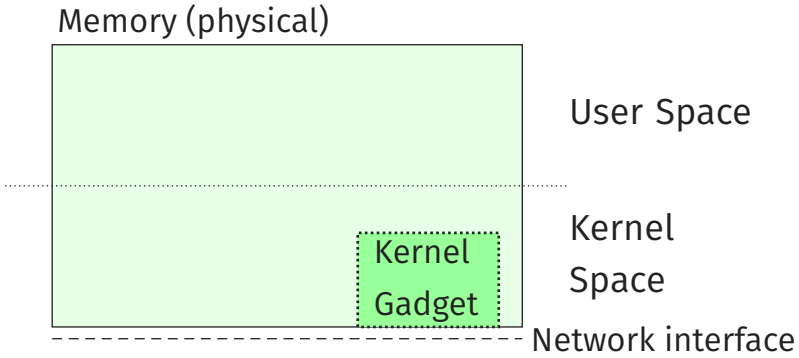

Memory (physical)
User Space
Kernel
Space
Network interface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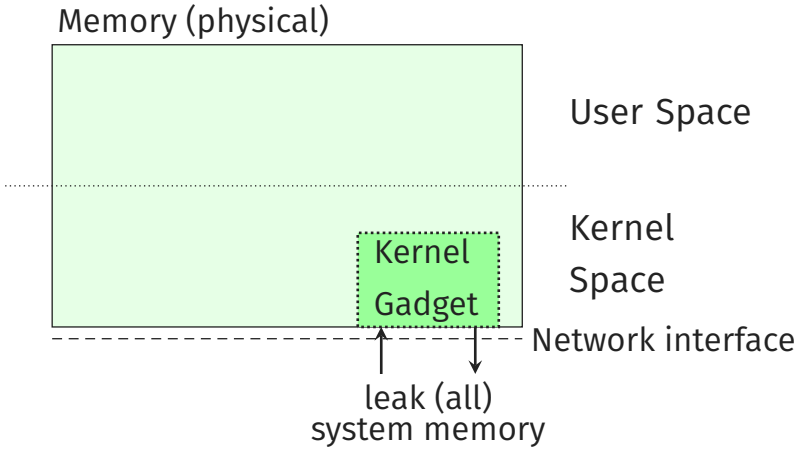
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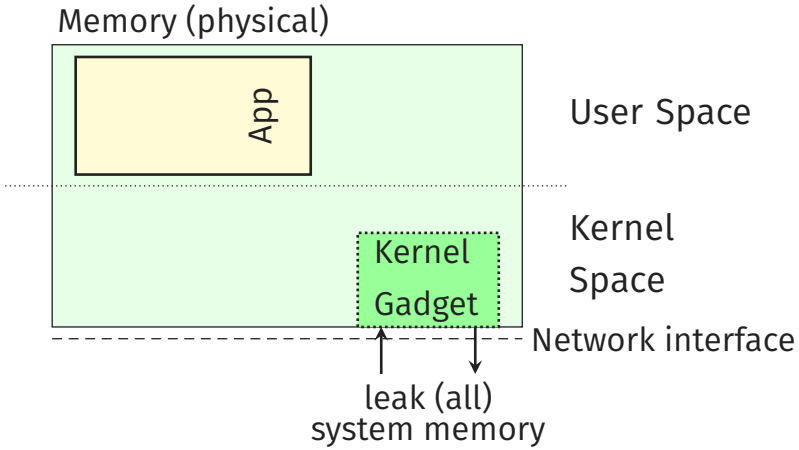
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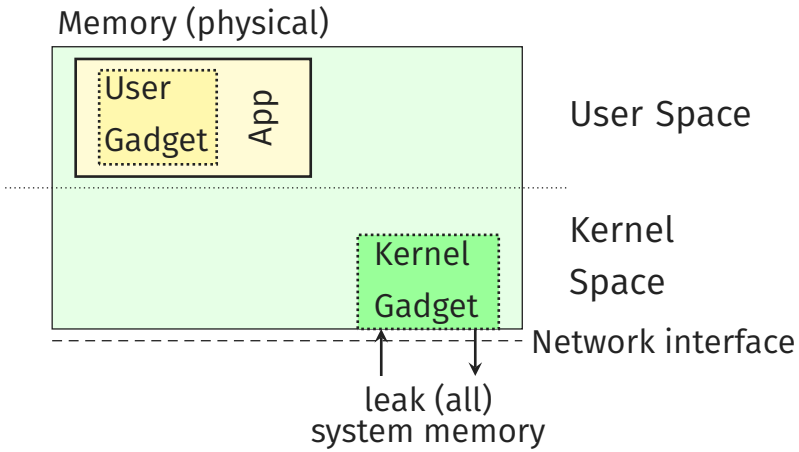
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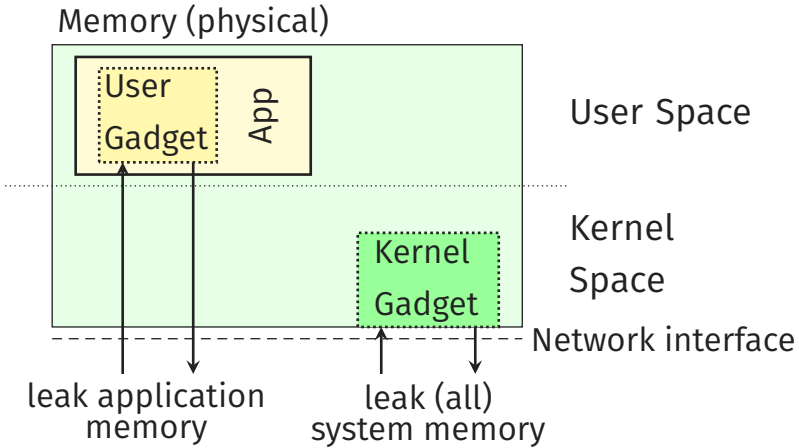
Memory (physical)
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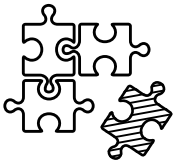
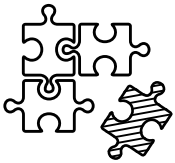


- Mistrain branch predictor with in-bounds requests

Combining Everything



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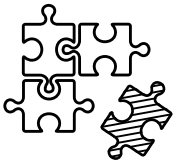

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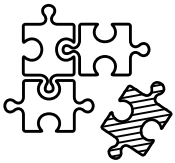

- Mistrain branch predictor with in-bounds requests
- Evict everything from cache via file download
- Leak a bit: do nothing (‘0’) or cache a memory location (‘1’)
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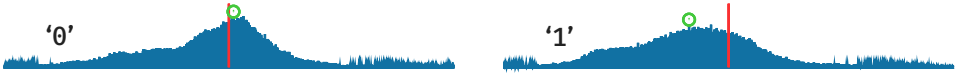
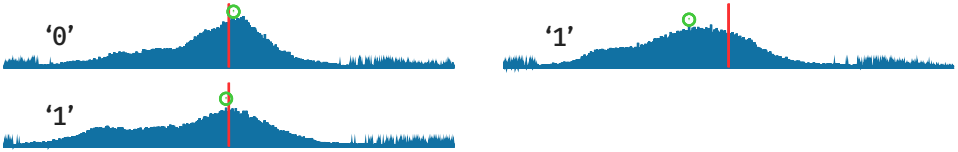
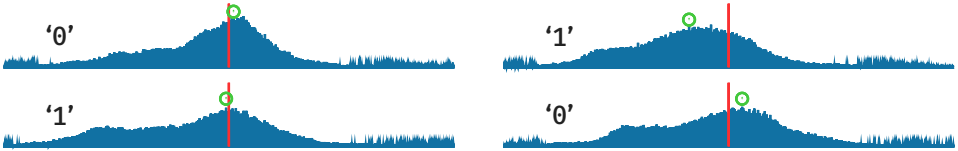
Leaking byte ’d’ (0)



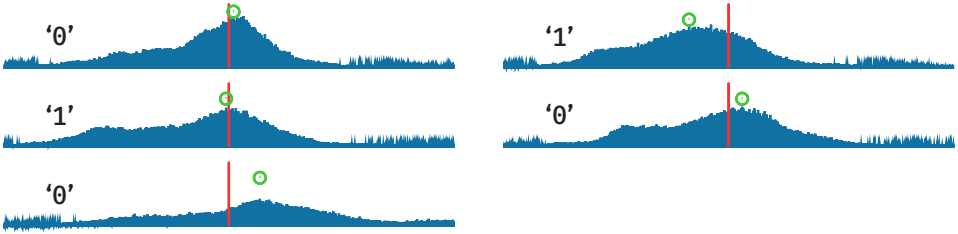
Leaking byte ’d’ (01)



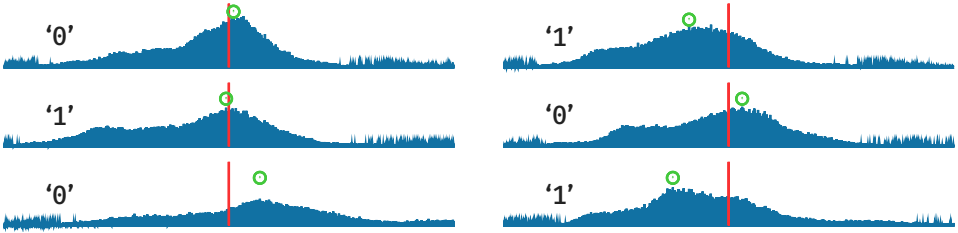
Leaking byte ’d’ (011)



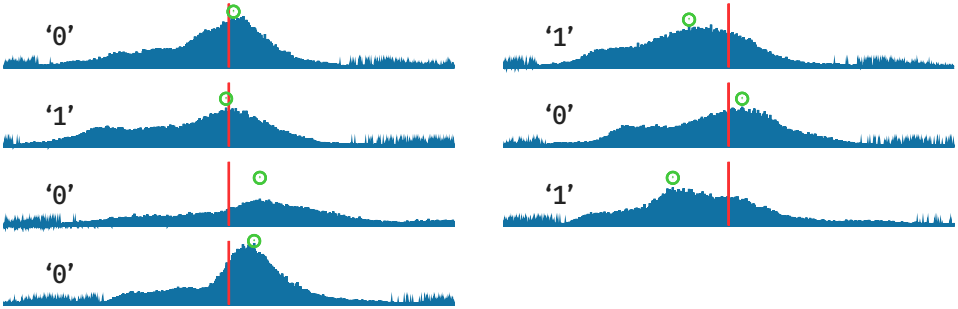
Leaking byte ’d’ (0110)



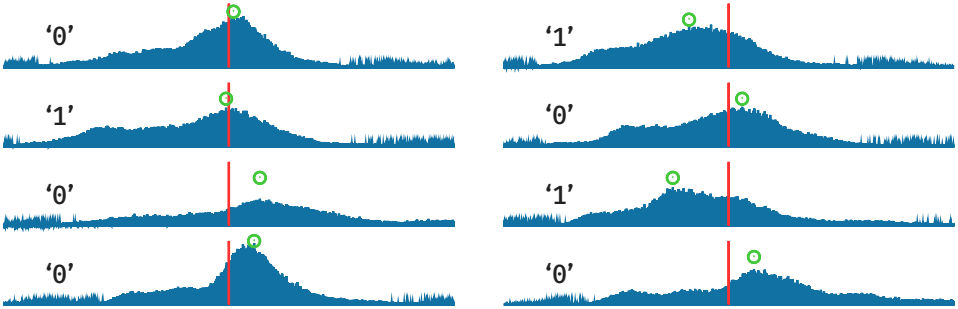
Leaking byte ’d’ (01100)



Leaking byte ’d’ (011001)



Leaking byte ’d’ (0110010)



Leaking byte ’d’ (01100100)

What can we exploit with them?

- Several possible attack targets

Attack Targets

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- Different impacts depending on target

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Web/FTP Servers
(user gadget)

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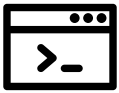

SSH Daemons
(user gadget)

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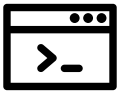

SSH Daemons
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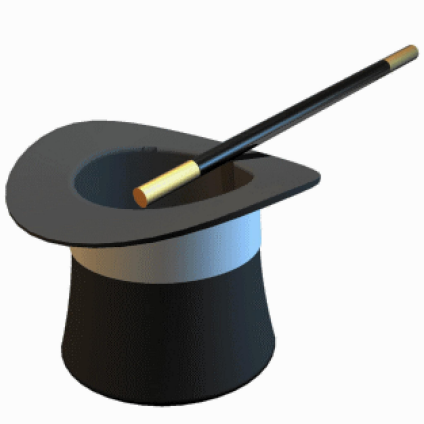
Network Drivers
(kernel gadget)



That’s nice but how do we find the gadgets?

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How to Find a Gadget

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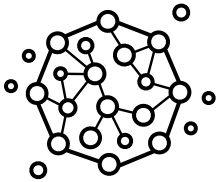
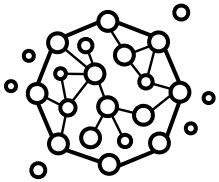
- Still no fully automated approach



- Linux kernel uses static code analysis



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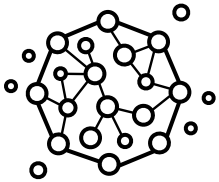

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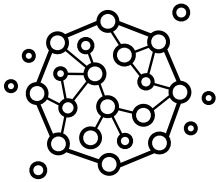

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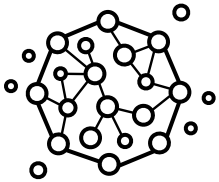

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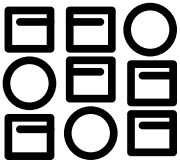

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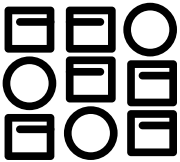

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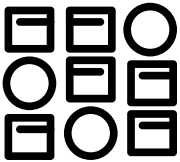

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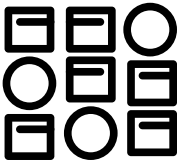

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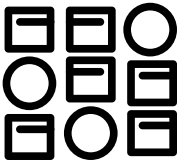

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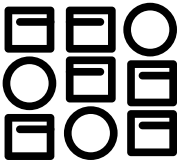
Automated Gadget Detection



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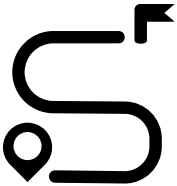
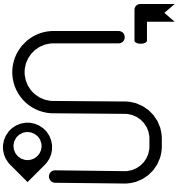


- Taint Tracking ↔ mark all input as evil



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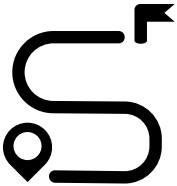

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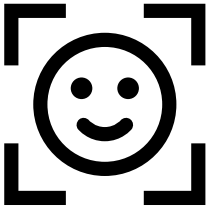
- $\exists$ a memory access relative within an array in a time window, report it as susceptible

Challenges in Identifying Gadgets



- Not clear how a Spectre gadget can look like

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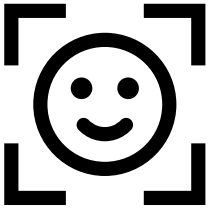

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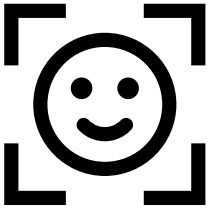

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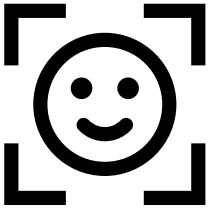

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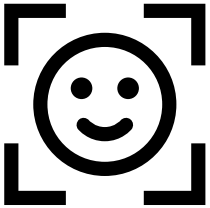

- Not clear how a Spectre gadget can look like
- Potentially many different forms
- Can be scattered over many instructions
- Similar to finding ROP chains
- While searching, discovered novel type of gadget

- No indirection, simple array access

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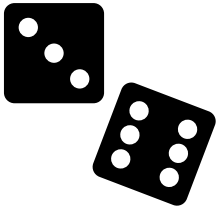
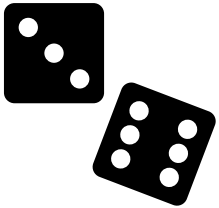
```
if (x < array_length)
  y = array[x];
```

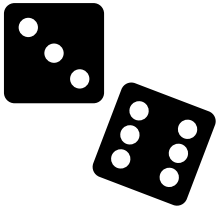


- What to do with weaker gadgets?



- What to do with weaker gadgets?

→ Break ASLR



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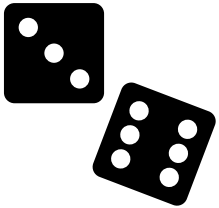
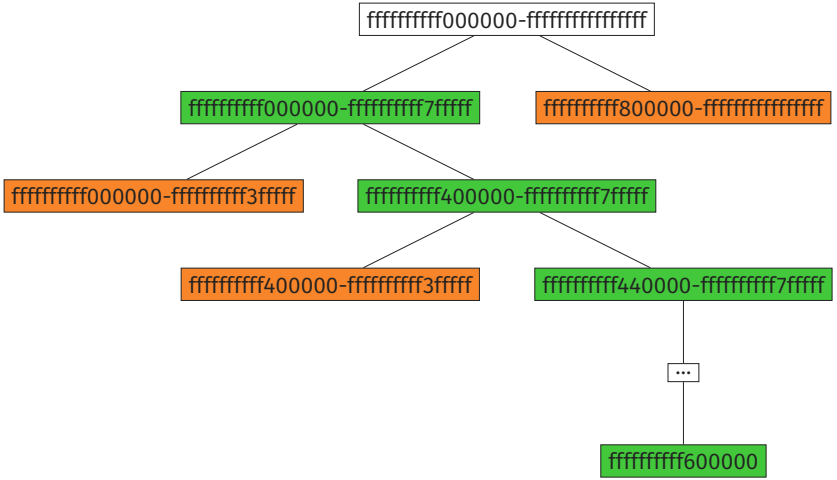
- Not relevant for local Spectre attacks



- What to do with weaker gadgets?

→ Break ASLR

- Not relevant for local Spectre attacks
- Valuable in a remote scenario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...
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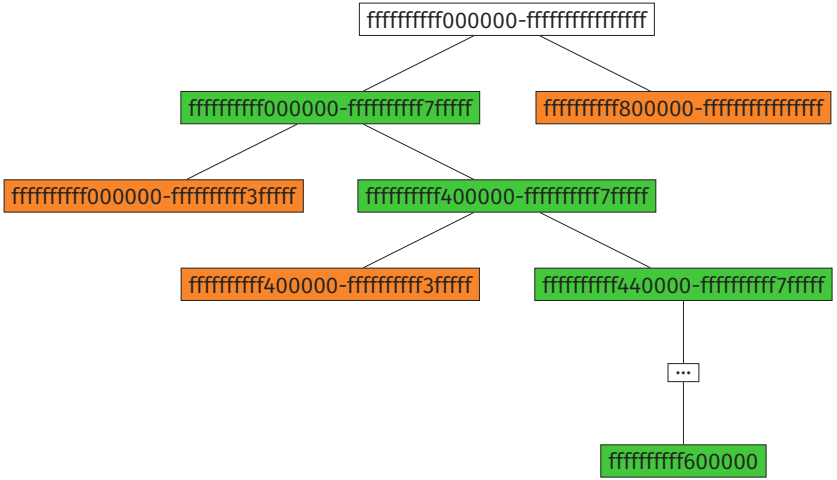
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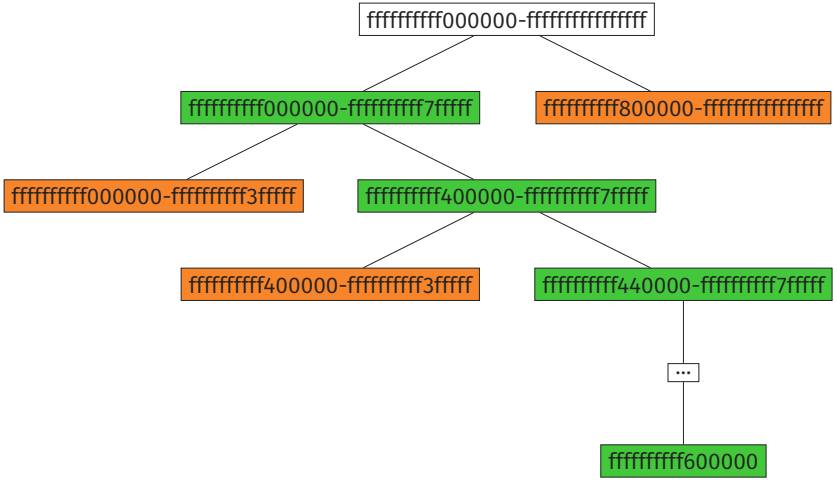
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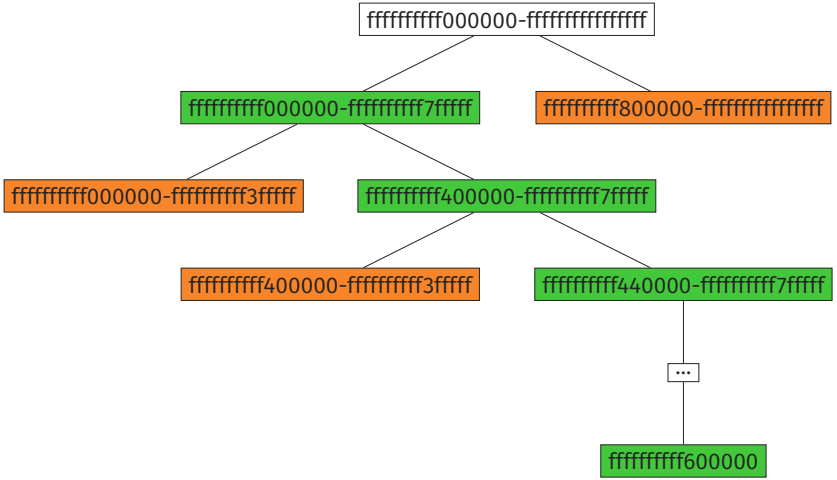
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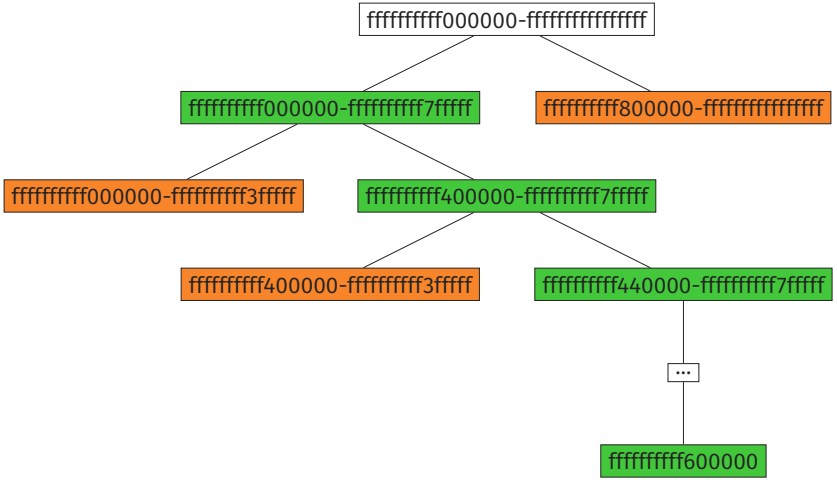
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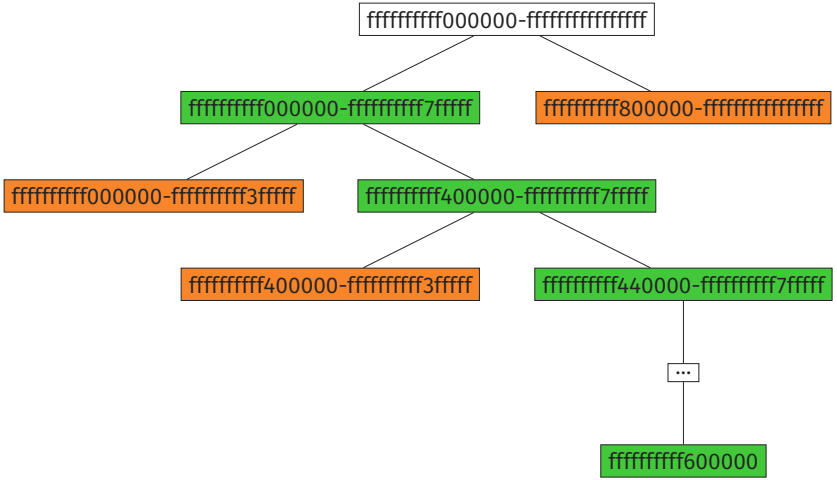
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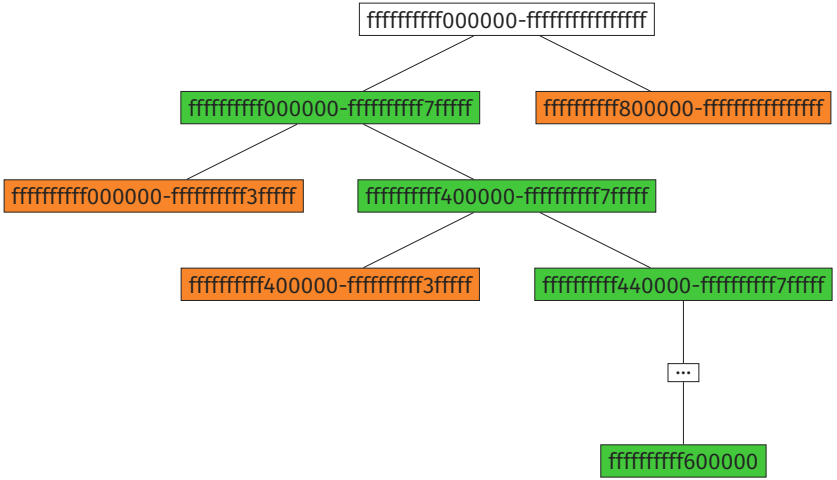
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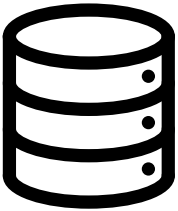
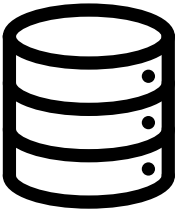
Is cache the only channel to exploit Spectre Remotely?

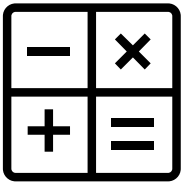
- All Spectre variants so far use the cache



- All Spectre variants so far use the cache
- Is this a requirement?

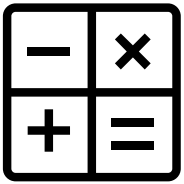


- All Spectre variants so far use the cache
- Is this a requirement?
- Can we encode the data somewhere else?



- Allow performing an operation in parallel on multiple data

Advanced Vector Instructions (AVX)



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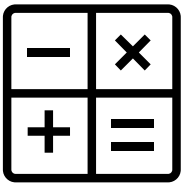

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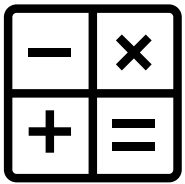

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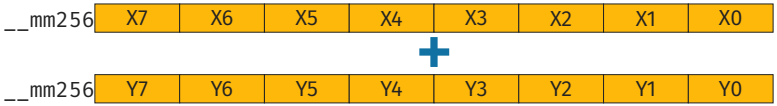

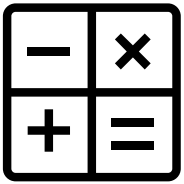

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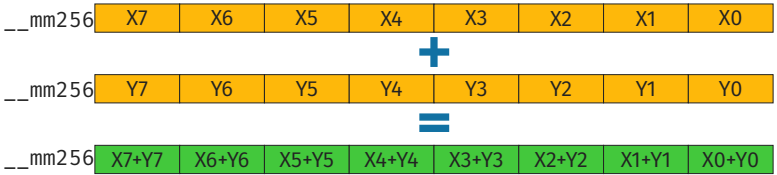

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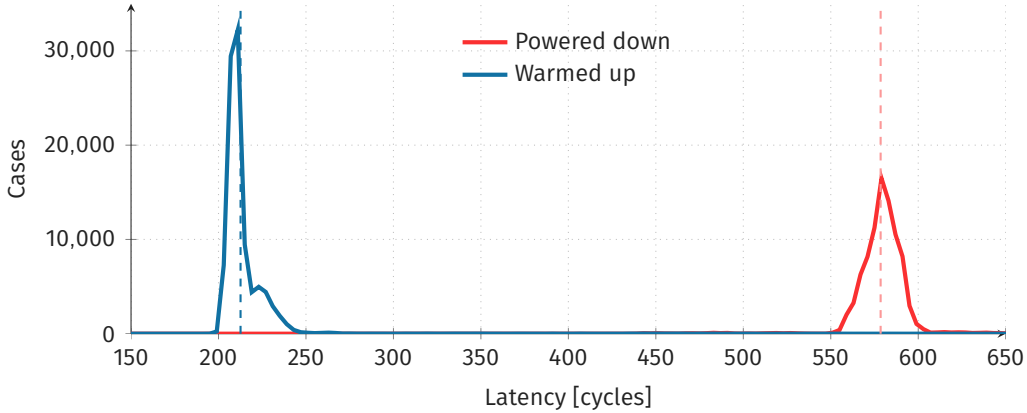
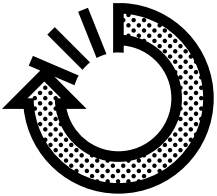
→ Leak timing information

AVX Latency


Powered down
Warmed up
Cases
30,000
20,000
10,000
0
150
200
250
300
350
400
450
500
550
600
650
Latency [cycles]

```
if (x < bitstream_length)
    if(bitstream[x])
        _mm256_instruction();
```



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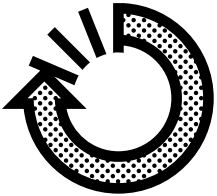

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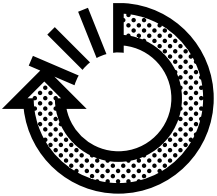
Resetting Microarchitectural State



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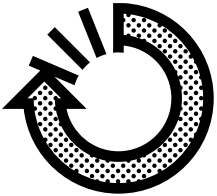

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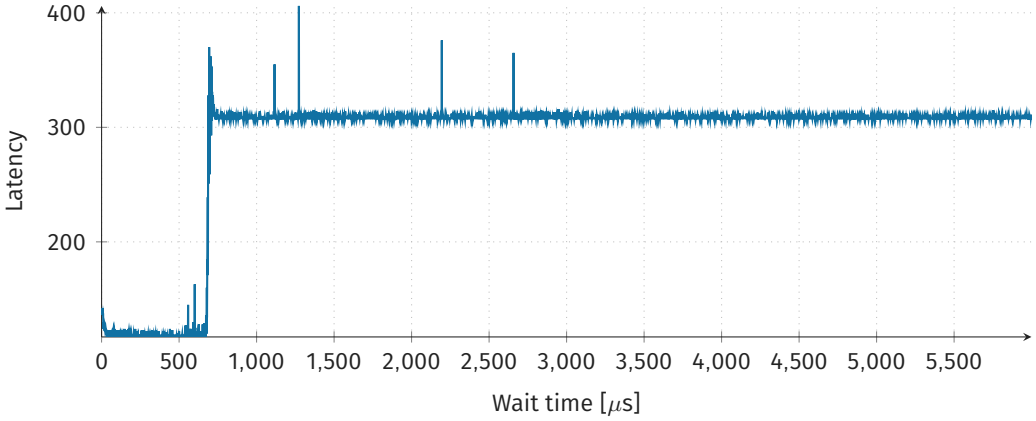
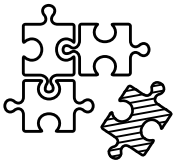
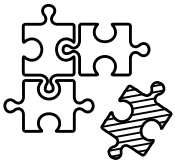
- $\rightarrow$ higher performance than cache covert channel

AVX Cooldown





1. Mistrain branch predictor with in-bounds requests



1. Mistrain branch predictor with in-bounds requests
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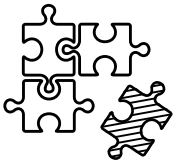

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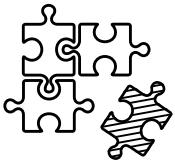

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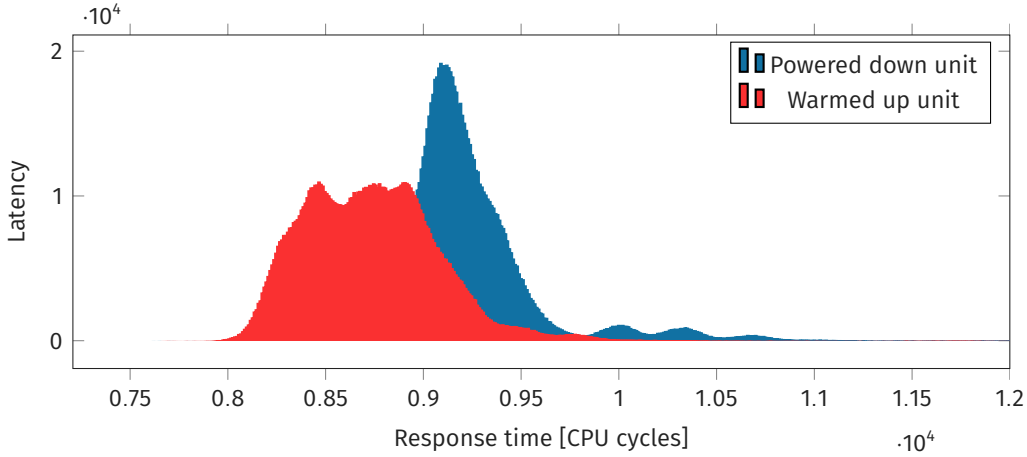
4. Measure function latency which uses AVX instruction


·10^4
2
1
0
Latency
Powered down unit
Warmed up unit
0.75
0.8
0.85
0.9
0.95
1
1.05
1.1
1.15
1.2
Response time [CPU cycles]
·10^4

Results

- NetSpectre tested in various environments

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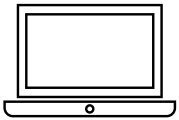

i5-6200U, i7-8550U

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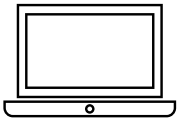

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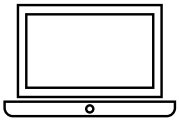

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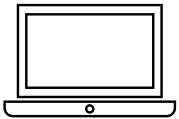

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ARM Cortex A75

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1 h/bit

How to prevent NetSpectre

- Mitigating NetSpectre

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Network side

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Network side

Fix Spectre

- Prevent NetSpectre on the network side

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Firewalls and DDoS protections

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Network segmentation

- Prevent (Net)Spectre on the system side

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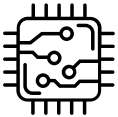

Hardware Fixes

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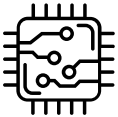
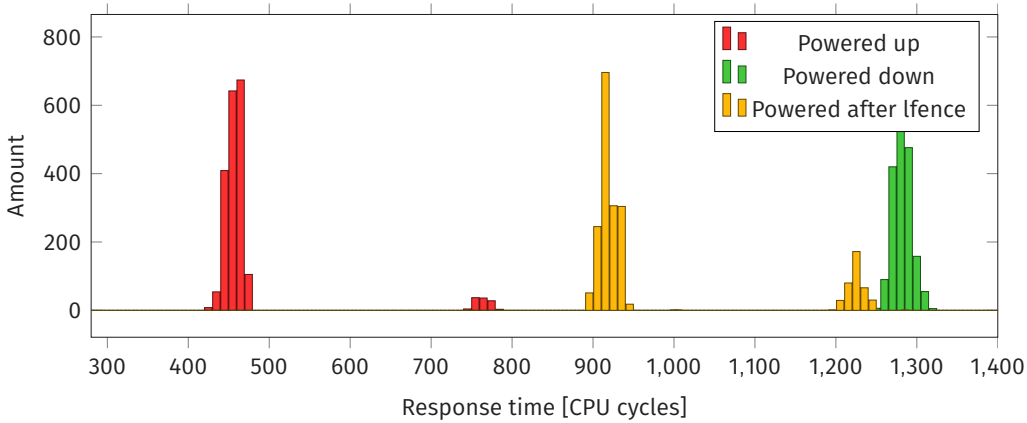


Hardware Fixes

Software Changes

AVX vs single lfence



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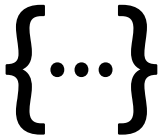
- Root problem has to be solved → more research required



- Speculative execution leaks secrets without exploiting bugs
- Spectre attacks are not limited to local attackers
- Spectre attacks have a larger impact than assumed

black hat ASIA 2019

NetSpectre

A Truly Remote Spectre Variant

Michael Schwarz @misc0110

Martin Schwarzl @marv0x90